Sulfur-Mini Development Kit
User Manual

Ver.1.0

Kondo Electronics Industry Co., Ltd.

Introduction

Thank you for purchasing a KEIm product.

Before using this product, please carefully read this manual and related documents, and use this product correctly while observing all precautions.

CAUTION

- The contents of this manual are subject to change without prior notice. Please contact Kondo Electronics Industry or refer to its website for the latest information before using the product.
- This product uses components intended for general electronic equipment. Do not use it in applications requiring extremely high reliability, such as aerospace, nuclear control systems, or life-support medical equipment.
- This product has been developed and manufactured for use in Japan. If this product, or any product incorporating it, is exported, the customer is responsible for complying with the Foreign Exchange and Foreign Trade Act and all other applicable export laws and regulations, and for completing all necessary procedures.
- Always turn off the power before connecting or disconnecting cables to connectors other than LAN and USB.
- Do not use this product in environments with high levels of water, humidity, dust, or oil smoke.
- Unauthorized use or reproduction, in whole or in part, of this product's related documents is prohibited.
- All company and product names mentioned in these manual and related documents are trademarks or registered trademarks of their respective companies.

Contact Information

- For inquiries about this product, please contact us at the email address below:

keim-support@kd-group.co.jp

Table of contents

1. Overview

This document describes the features and specifications of the “Sulfur Mini Development Kit” based on the Agilex™ 5 SoC FPGA E-Series.

1.1. Package Contents

This product package includes the following items.
Before use, please confirm that all items are included.

- 1 x SoM and Carrier Board (assembled)
- 1 x Heat Sink (evaluation sample)

1.2. Required Items (Not Included)

To use this product, prepare the following equipment and environment:

- USB Power Delivery AC Adapter
  Output: 45 W or higher (15 V / 3 A)
  Recommended model: ACDC-PD8445BK (ELECOM)
  https://www.elecom.co.jp/products/ACDC-PD8445BK.html
- microSD card
  Capacity: 32 GB or higher recommended
  Recommended model: KLMEA032G (KIOXIA)
  https://www.kioxia.com/ja-jp/personal/support/download/micro-sd/exceria/klmea.html
- RTC backup battery
  Recommended model: CR1220 (Panasonic)
  https://energy.panasonic.com/jp/business/products/lithium/coin-cr-standard/models/CR1220
- Altera FPGA Download Cable II or III
  Recommended model: PL-USB2-BLASTER or PL-UB3-CABLE
  https://docs.altera.com/r/docs/864466/current/usb-blaster-iii-fpga-development-cable-user-guide
- UART Terminal Cable
  Specification：Type-A to Type-C
  Recommended model: U2C-AC10BK
- PC
  Quartus® Prim Pro Edition Version 25.3.1 or later is used as the development tool.
  For PC system requirements, refer to the official website of Altera.

1.3. **Product Features**

This product is a development kit that uses the “KEIm-A5ESoM Mini“ (Kondo Electronics Industry), a System-on-Module (SoM) equipped with the Agilex™ 5 SoC FPGA E-Series.
The carrier board provides various peripheral interfaces such as MIPI, Ethernet, USB 2.0, as well as expansion interfaces including an FMC connector and a 2 x 20 pin header.

This product provides a platform that enables hardware and software developers to quickly start system development and functional evaluation using the Agilex™ 5 SoC FPGA E-Series.

The main features of this product are as follows:

(1) Configuration Using a Compact SoM
This product adopts the compact SoM “KEIm-A5ESoM Mini” as its core component.
After evaluating the device and verifying functions using this product, the SoM can be used directly as the core module in actual product designs.
This helps improve hardware development efficiency and reduce development time.

(2) Rich Expansion Interfaces
The board is equipped with an FMC connector and a 2 x 20 pin header, allowing connection of commercially available expansion boards such as FMC (FPGA Mezzanine Card) and Raspberry Pi HATs.
This enables flexible evaluation of various interface functions and application development.

(3) Compact From Factor
This product is designed with a compact form factor, making it suitable not only for evaluation purposes but also for integration into prototype systems.

(4) Provision Reference Designs
This product will provide hardware and software reference designs for utilizing the onboard peripheral interfaces.
This allows developers to efficiently start application development using the Agilex™ 5 SoC FPGA E-Series.

1.4. Precautions for Use

When using this product, see the following precautions:

- When connecting FMC modules or Raspberry Pi HAT modules to this product, ensure that the specifications of the modules and the corresponding port on this product match. Verify compatibility in terms of signal levels, power specifications, and connection methods before making the connection.

- When handling this product, take appropriate ESD (Electrostatic Discharge) precautions to prevent damage caused by static electricity.

- Proper power supply and thermal design are required for stable operation of this product. Pay close attention to power capacity and thermal considerations during system design.

- Four specific screw holes inside the heat spreader are provided for evaluation purposes only.
  As the heat spreader is designed with priority on thin and lightweight form factor, the strength of these screw holes is not sufficient. Therefore, mechanical strength is not guaranteed for use in production applications.
  In addition, as these screw holes are through holes, use screws with a protrusion length of 3 mm or less to prevent contact with the board.

- Signals connected to the TPM are assigned to the LPDDR4 bank I/O of the SoM. Due to the specifications of the SoC FPGA EMIF, this function cannot be used when the HPS F2H bridge is enabled. When using this function, set the HPS F2H bridge to disabled.

1.5. Product Specifications

The specifications of this product are shown below.

Figure 1-1 Product Specifications

Item		Description
SoM		KEIm-A5ESoM Mini (CS1 version)
	SoC FPGA	Agilex™ 5 SoC FPGA E-Series, M16A package: A5ED013BM16AI4SCS Hard Processor System (HPS): Dual-core Arm Cortex-A76 (up to 1.4 GHz), Dual-core Arm Cortex-A55 (up to 1.25GHz) FPGA Fabric: 138,060 LEs
	Memory	LPDDR4 SDRAM 4GB (1G x 32-bit)
	Configuration ROM	QSPI Flash 1Gbit
	Storage Device	eMMC 32GB*1
Ethernet		Gigabit Ethernet port PHY: KSZ9131RNX (Microchip)
USB 2.0		USB 2.0 High-Speed Type-A (Host) connectors x2 Hub: USB2422-I/MJ (Microchip) PHY: USB3320C-EZK (Microchip)
SDMMC		microSD card slot*1
MIPI		22-pin connectors x 2 Connector for Bank 3A: 4-lane (fixed at 1.1 V) Connector for Bank 2A: 4-lane
Clock		4 x crystal oscillators for SoC FPGA 100 MHz for HPS 100 MHz for FPGA MIPI reference clock 25 MHz x 2
USB-UART		USB Type-C connector x 1 USB-to-UART bridge: FT232RN (FTDI)
RTC		DS1339A (ADI)
EEPROM		24AA64 (Microchip)
Debug I/F		JTAG 10-pin connector
FAN Power Connector		4-pin: BM04B-PASS-1 (JST)
FMC Connector		400-pin HPC connector: ASP-134486-01 (Samtec) Transceiver x 4 lanes Up to 72 single-ended (1.3V / 1.2V) or 36 differential pairs
2 x 20 Pin Header		2.54 mm pitch pin header 26 x 3.3 V I/O (2 shared with I2C)
Others		DIP switches x4, push switches x4, LEDs x4
Input Power		Supplied from +15V via USB-PD
Power Consumption		TBD
Operating Temperature		0°C~ +40°C
Dimensions		110 × 110 x 18.4mm (excluding heat sink and protrusions)

*1 The eMMC and microSD card are mutually exclusive and cannot be used simultaneously.

1.6. **Block Diagram**

This block diagram of this product is shown below.

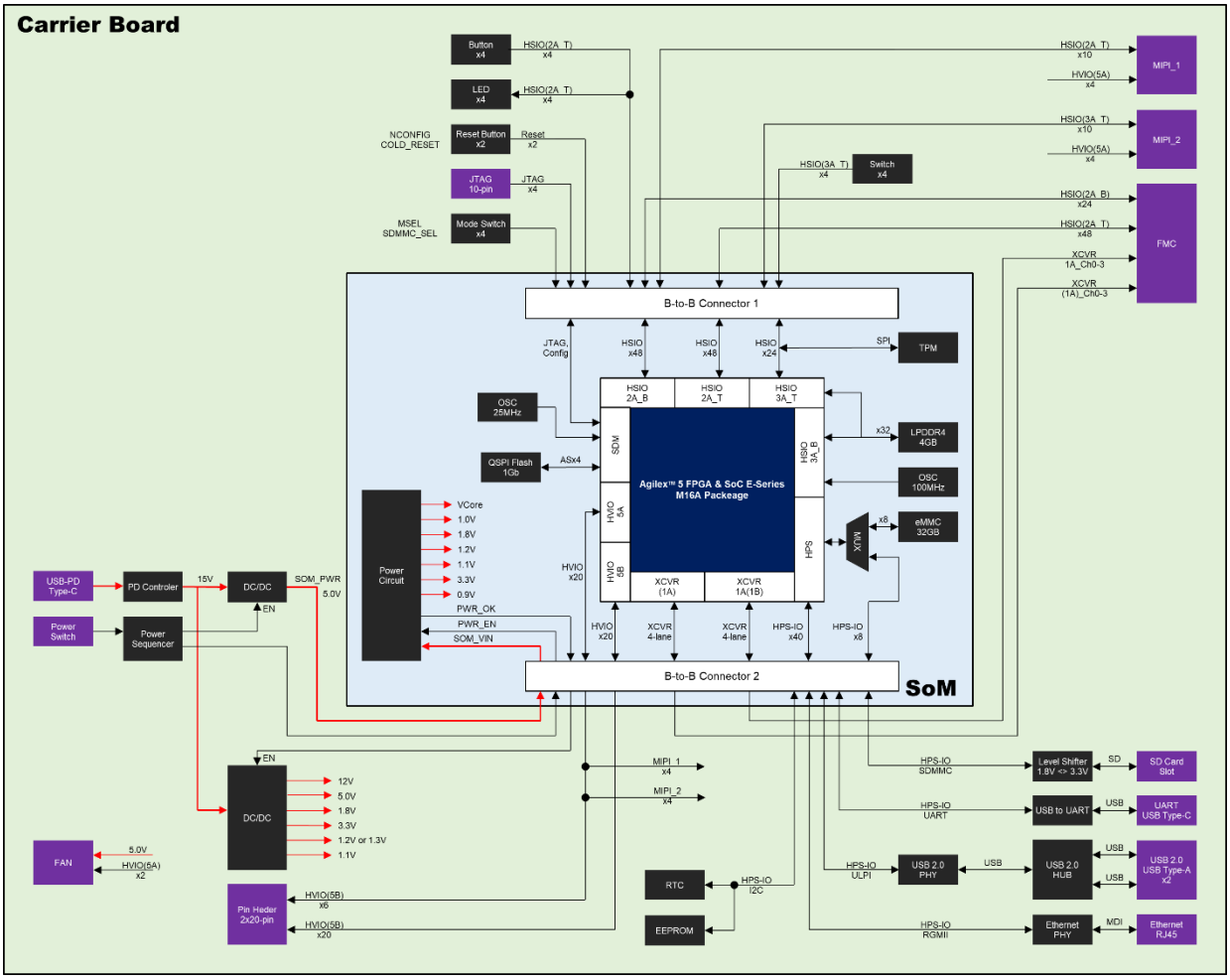


Figure 1-2 Sulfur-Mini Development Kit Block Diagram

1.7. **Board Layout**

The board layout and the main components of this product are shown below.

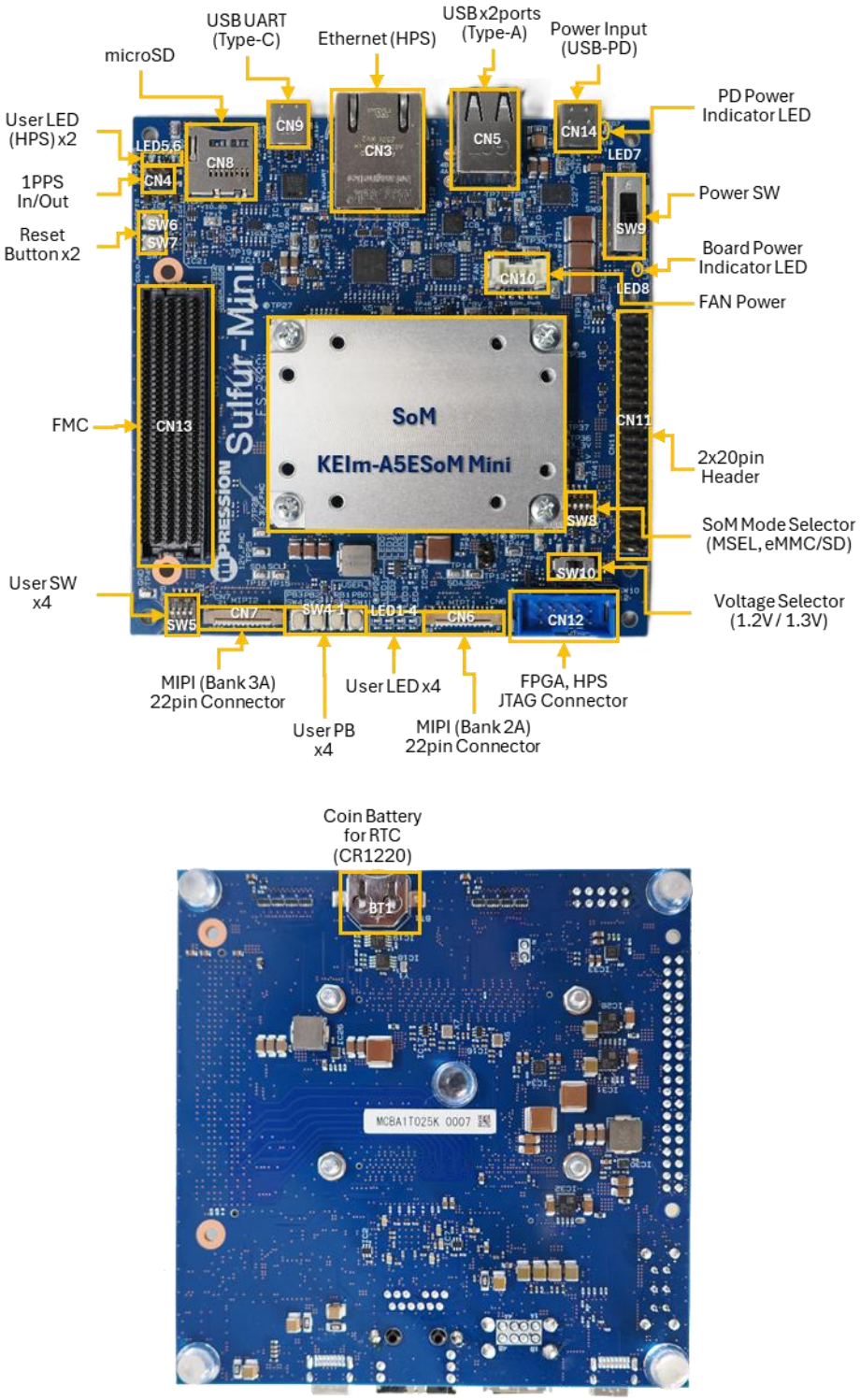


Figure 1-3 Board Layout

Table 1-1 List of Main Components

Reference	Name	Description
SoM		
SoM	KEIm-A5ESoM Mini	Agilex™ 5 SoC FPGA E-Series M16A package (A5ED013BM16AI4SCS)
I/F Connector		
CN1, CN2	Board-to-Board Connectors	240-pin, 0.635 mm pitch, 4-row board-to-board connectors Carrier board: ADM6-60-01.5-L-4-2-A (Samtec) SoM: ADF6-60-03.5-L-4-2-A (Samtec)
CN3	Ethernet Port	RJ45 connector with integrated magnetics
CN5	USB 2.0 Connector	Type-A high speed, 2-port connector
CN6	MIPI Connector 1	22-pin 0.5 mm pitch FFC connector, 4-lanes
CN7	MIPI Connector 2	22-pin 0.5 mm pitch FFC connector, 4-lanes, fixed at 1.1 V
CN8	microSD Card Slot	Connected to HPS SDMMC
CN9	USB-UART Connector	USB Type-C
CN10	FAN Connector	4-pin, 5 V output
CN11	2 x 20 Pin Header	2.54 mm pitch, 40 pins, 26 x 3.3 V HVIO (2 shared with I2C)
CN12	JTAG Connector	2.54 mm pitch, 10 pins, 1.8 V
CN13	FMC Connector	400-pin (HPC), connected HSIO Up to 72 single-ended or 36 differential pairs Transceivers x 4 lanes
CN14	Power Connector	USB Type-C, USB-PD
Battery Holder		
BT1	Battery Holder	For RTC backup (CR1220)
Switches		
SW1, SW2, SW3, SW4	User Push Switches	All connected to HVIO
SW5	User DIP Switches	4 positions, all connected to HVIO
SW6	Reset Switch	For reconfiguration
SW7	Reset Switch	For HPS reset
SW8	SoM Mode Switch	Used for FPGA configuration mode setting and storage device selection
SW9	Power Switch	Turns board power ON / OFF
SW10	HSIO_2A Voltage Select Switch	Selects VCCIO (1.2 V / 1.3 V) for Bank 2A (HSIO)
LEDs		
LED1, LED2, LED3, LED4	User LEDs (FPGA)	Connected to HVIO
LED5, LED6	User LEDs (HPS)	Connected to HPS I/O
LED7	PD Power Status LED	Turns on when 15 V is supplied via USB-PD
LED8	Board Power Status LED	Turns on when power switch is ON and board is powered

2. Functional Specifications

This section describes the details of the various functions provided by this product.

2.1. SoM (KEIm-A5ESoM Mini)

The basic specifications of the SoM (KEIm-A5ESoM Mini) mounted on this product are shown below.

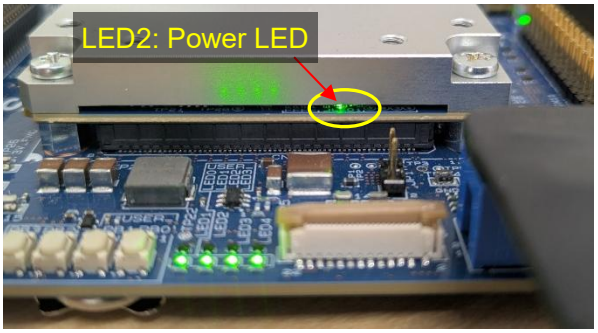
For more details, refer to the KEIm-A5ESoM Mini Hardware Manual.

Table 2-1 SoM Basic Specifications

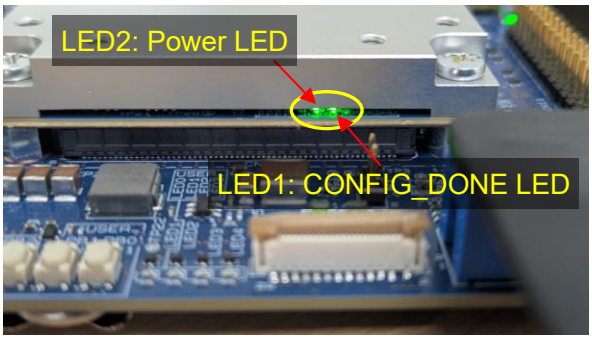
Item		Description
SoC FPGA		Agilex™5 SoC FPGA E-Series
	Device	A5ED013BM16AI4SCS
	Processor	Dual-core Arm Cortex-A76 up to 1.4 GHz Dual-core Arm Cortex-A55 up to 1.25GHz
	Logic Elements	138,060 LEs
	M20K memory blocks	358 blocks
	MLAB memory count	2,340 counts
	I/O PLL	4
	Fabric-feeding I/O PLL	8
	Variable-precision DSP blocks	188
	18 x 19 multipliers	376
Memory		32-bit, 4GB LPDDR4 SDRAM
Configuration ROM		1Gbit QSPI Flash
Storage Device		32GB eMMC
TPM Module		SLB9672XU20FW1612XTMA1 (Infineon)
Clock	OSC (SDM)	25 MHz fixed clock
	OSC (LPDDR4)	100 MHz fixed clock
Board-to-Board Connectors		240-pin connectors x 2
	Part Number	ADF6-60-03.5-L-4-2-A (Samtec)
	HPS I/O	Up to 48 pins (RGMII x1, ULPI x1, UART x1, I2C x1, SDMMC x1, GPIOs)
	HSIO	Up to 96 pins
	HVIO	Up to 40 pins
	Transceiver (17Gbps)	4 lanes
	Debug I/F	JTAG
Input Power		4.7V to 13.2V
Current Consumption		TBD
Operating Temperature Range		-45°C to +85°C
Dimensions		60 × 43 x 10 mm (including heat spreader)

2.1.1. **SoM Status LEDs**

This product is equipped with status LEDs for system monitoring. The functions of each LED are described below.



(a) Not configured



(b) Configuration complete

Table 2-2 SoM Status LEDs

Reference	Nam	Description
SoM : LED1	CONF_DONE LED	Indicates the configuration status. ON: Configuration completed OFF: Configuration not completed
SoM : LED2	Power LED	Indicates the power input status. This LED turns ON when power is supplied.

2.2. **Board-to-Board Connectors**

The board layout of the board-to-board connectors used for connection to the SoM is shown below.

For the pin assignments of each connector, refer to the KEIm-A5ESoM Mini Hardware Manual.

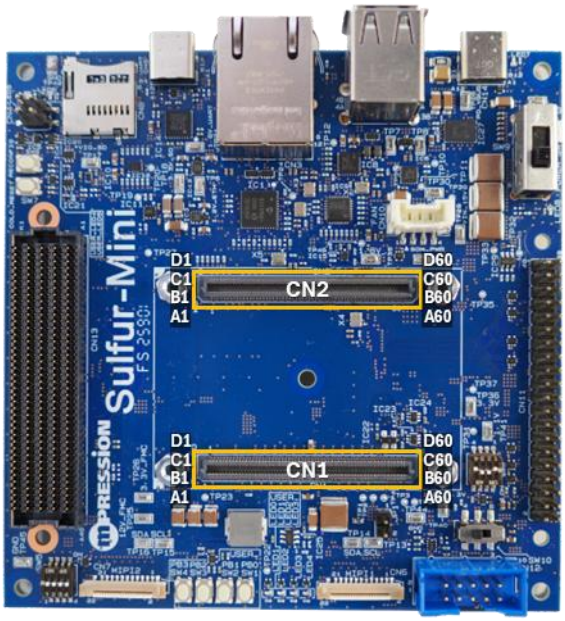


Figure 2-1 SoM Connector Layout

2.3. **Switches and LEDs**

The board layout of the switches and LEDs on this product is shown below.

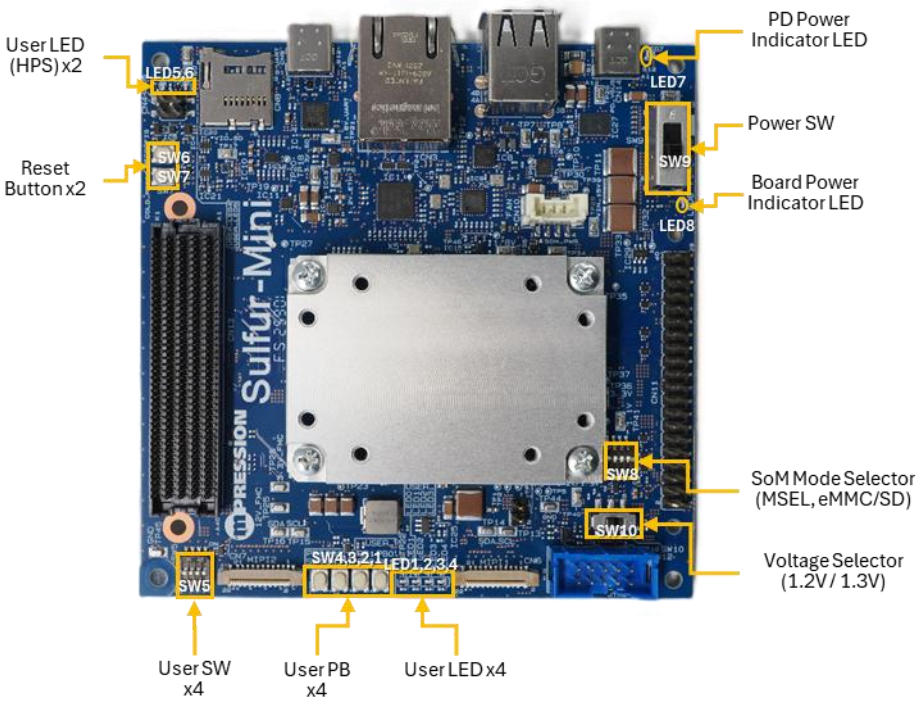


Figure 2-2 Switch and LED Layout

Table 2-3 List of Switches and LEDs

Reference	Name	Description
SW1, SW2, SW3, SW4	User Push Swtiches	Push switches for user operation. For details, refer to Selection 2.3.2, User Push Switches.
SW5	User DIP Switch	DIP switch for user configuration. For details, refer to Selection 2.3.3, User DIP Switch.
SW6	Reset Switch (Reconfiguration)	Reconfigures the FPGA.
SW7	Reset Switch (COLD_RESET)	Cold reset for the HPS.
SW8	SoM Mode Switch	Sets the FPGA operation mode and boot memory. For details, refer to Selection 2.3.4, SoM Mode Switch.
SW9	Power Switch	Slide switch for board power ON/OFF.
SW10	HSIO_2A Voltage Select Switch	Selects the power voltage for the HSIO_2A bank. For details, refer to Selection 2.3.5, HSIO_2A Voltage Select Switch.
LED1, LED2, LED3, LED4	User LEDs (FPGA)	LED for user control. For details, refer to Selection 2.3.1, User LEDs.
LED5, LED6	User LED (HPS)	LED for user control. For details, refer to Selection 2.3.1, User LEDs.
LED7	PD Power Status LED	Turns on when 15 V is supplied via USB-PD.
LED8	Board Power Status LED	Turns on when the power switch is ON and the board is powered.

2.3.1. **User LEDs**

The circuit, pin assignments, and display behavior of the user LEDs are shown below.

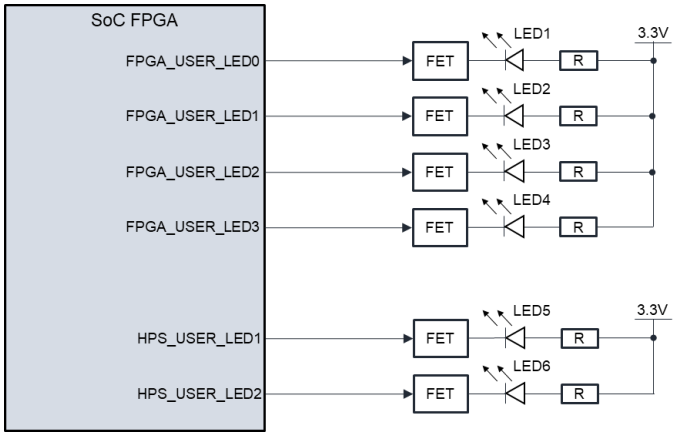


Figure 2-3 User LED Circuit

Table 2-4 User LED Circuit Pin Assignment

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
FPGA_USER_LED0	CN1.B35	HSIO_2A_B_IO1_N	Y5	1.2-V or 1.3-V LVCMOS*1
FPGA_USER_LED1	CN1.B36	HSIO_2A_B_IO1_P	W4	1.2-V or 1.3-V LVCMOS*1
FPGA_USER_LED2	CN1.C34	HSIO_2A_B_IO2_N	AA3	1.2-V or 1.3-V LVCMOS*1
FPGA_USER_LED3	CN1.C35	HSIO_2A_B_IO2_P	Y4	1.2-V or 1.3-V LVCMOS*1
HPS_USER_LED1	CN2.D12	HPS_IOA11_1V8	A23	1.8-V LVCMOS
HPS_USER_LED2	CN2.D11	HPS_IOA12_1V8	A26	1.8-V LVCMOS

Table 2-5 User LED Indication

Reference	Name	Description
LED0	FPGA_USER_LED0	Turns off when the signal is Low (logic 0) and turns on when signal is High (logic 1).
LED1	FPGA_USER_LED1	Turns off when the signal is Low (logic 0) and turns on when signal is High (logic 1).
LED2	FPGA_USER_LED2	Turns off when the signal is Low (logic 0) and turns on when signal is High (logic 1).
LED3	FPGA_USER_LED3	Turns off when the signal is Low (logic 0) and turns on when signal is High (logic 1).
LED4	HPS_USER_LED1	Turns off when the signal is Low (logic 0) and turns on when signal is High (logic 1).
LED5	HPS_USER_LED2	Turns off when the signal is Low (logic 0) and turns on when signal is High (logic 1).

*1 Adjust these IO Standard settings to match the voltage applied to HSIO_2A, as configured by SW10 (HSIO Voltage Select Switch).

2.3.2. **User Push Switches**

The circuit, pin assignments, and switch functions of the user push switches on this product are shown below.

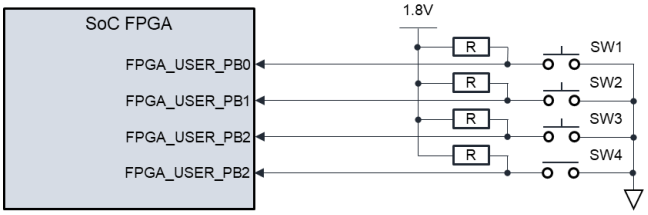


Figure 2-4 User Push Switches Circuit

Table 2-6 Pin Assignments of User Push Switch Circuit

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
FPGA_USER_PB0	CN1.C37	HSIO_2A_B_IO3_N	AA4	1.2-V or 1.3-V LVCMOS*1
FPGA_USER_PB1	CN1.C38	HSIO_2A_B_IO3_P	AB3	1.2-V or 1.3-V LVCMOS*1
FPGA_USER_PB2	CN1.A34	HSIO_2A_B_IO4_N	AC3	1.2-V or 1.3-V LVCMOS*1
FPGA_USER_PB3	CN1.A35	HSIO_2A_B_IO4_P	AB4	1.2-V or 1.3-V LVCMOS*1

Table 2-7 User Push Switch Functions

Reference	Name	Description
SW1	FPGA_USER_PB0	Low level (logic 0) when pressed; High level (logic 1) when not pressed
SW2	FPGA_USER_PB1	Low level (logic 0) when pressed; High level (logic 1) when not pressed
SW3	FPGA_USER_PB2	Low level (logic 0) when pressed; High level (logic 1) when not pressed
SW4	FPGA_USER_PB3	Low level (logic 0) when pressed; High level (logic 1) when not pressed

*1 Adjust these IO Standard settings to match the voltage applied to HSIO_2A, as configured by SW10 (HSIO Voltage Select Switch).

2.3.3. **User DIP Switch**

The circuit, pin assignments, and switch functions of the user DIP switches on this product are shown below.

User Restrictions

The following restrictions apply when using these switches:

- These switches are assigned to the LPDDR4 bank of the SoM.
- Due to the EMIF specifications of the SoC FPGA, these switches cannot be used when the HPS F2H bridge is enabled.

When using these switches, disable the HPS F2H bridge.

Notes on FPGA Configuration

No pull-up resistors are mounted on the carrier board for these switches.

Therefore, it is necessary to enable the weak pull-up setting in the FPGA configuration.

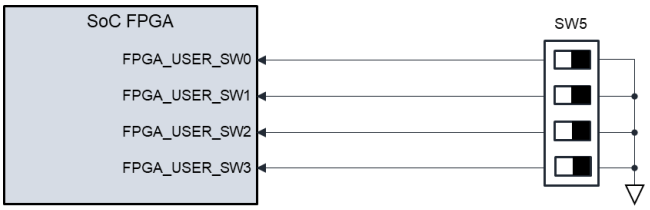


Figure 2-5 User DIP Switch Circuit

Table 2-8 Pin Assignments of User DIP Switch Circuit

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
FPGA_USER_SW0	CN1.D8	HSIO_3A_T_IO13_N	L1*1	1.1-V
FPGA_USER_SW1	CN1.D9	HSIO_3A_T_IO13_P	M1*1	1.1-V
FPGA_USER_SW2	CN1.D5	HSIO_3A_T_IO14_N	K1*1	1.1-V
FPGA_USER_SW3	CN1.D6	HSIO_3A_T_IO14_P	L2*1	1.1-V

Table 2-9 User DIP Switch Functions

Reference	Name	Description
SW13.1	FPGA_USER_SW0	Low level (logic 0) when ON; High level (logic 1) when OFF
SW13.2	FPGA_USER_SW1	Low level (logic 0) when ON; High level (logic 1) when OFF
SW13.3	FPGA_USER_SW2	Low level (logic 0) when ON; High level (logic 1) when OFF

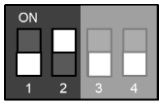
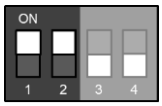
*1 Since no external pull-up resistors are provided, enable the weak pull-up in the pin settings before use.

2.3.4. **SoM Mode Switch**

This product is equipped with switches for configuring the operating mode of the SoM.

The functions of each switch are described below.

Table 2-10 SoM Mode Switch

<table>
<tr><th>Reference</th><th>Name</th><th>Description</th></tr>
<tr><td>SW8.1</td><td>MSEL1</td><td rowspan="2">Configuration mode*1 selection
<table>
<tr><th>Mode</th><th>MSEL1</th><th>MSEL2</th><th>Figure</th></tr>
<tr><td>JTAG only mode (default)</td><td>OFF</td><td>OFF</td><td> 
</td></tr>
<tr><td>AS Normal mode</td><td>OFF</td><td>ON</td><td> 
</td></tr>
<tr><td>AS Fast mode</td><td>ON</td><td>ON</td><td> 
</td></tr>
</table></td></tr>
<tr><td>SW8.2</td><td>MSEL2</td></tr>
<tr><td>SW8.3</td><td>SDMMC_SEL</td><td>Storage device selection
ON: SD mode (default)
OFF: eMMC mode</td></tr>
<tr><td>SW8.4</td><td>Reserved</td><td>-</td></tr>
</table>

*1 For details on the configuration modes ,refer to the Agilex™5 FPGA & SoC E-Series documentation.

2.3.5. **HSIO_2A Voltage Select Switch**

This product is equipped with a switch for selecting the supply voltage of HSIO bank 2A.

The circuit and switch settings are shown below.

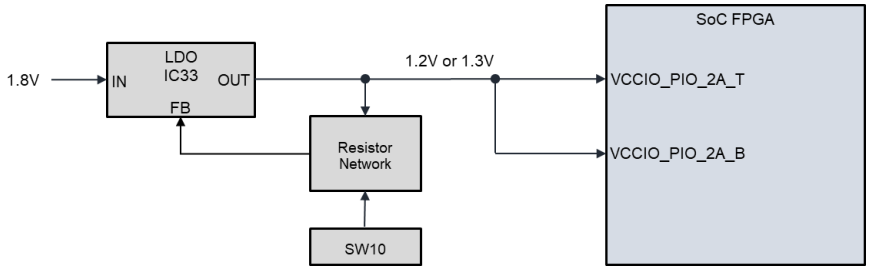
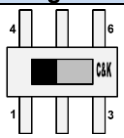
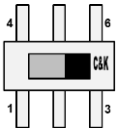


Figure 2-6 HSIO_2A Voltage Selection Circuit

Table 2-11 HSIO_2A Voltage Select Switch Settings

Reference	Name	Description	Figure
SW10	HSIO_2A_VCCIO	Slider set to pins 1-4 side: Sets the HSIO_2A bank voltage to 1.2 V (default)	
		Slider set to pins 3-6 side: Sets the HSIO_2A bank voltage to 1.3 V	

2.4. **Power Circuit**

The power circuit of this product is shown below.

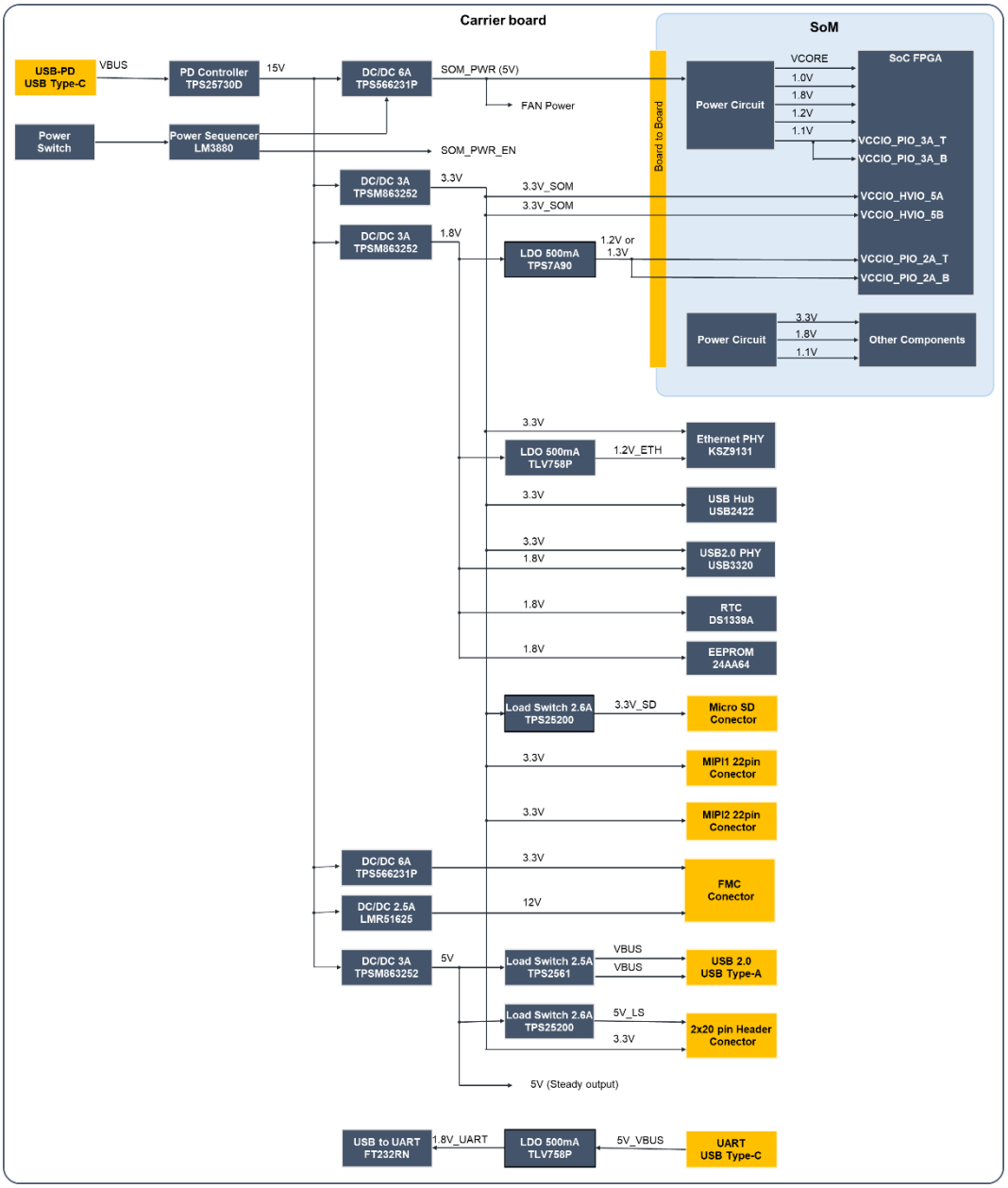


Figure 2-7 Power Circuit

2.5. Configuration Circuit

The configuration circuit of this product is shown below.

Configuration can be performed via the JTAG connector or from the QSPI flash on the SoM.

The configuration mode can be selected using the SoM Mode Switch. For details on the SoM Mode Switch, refer to Selection 2.3.4.

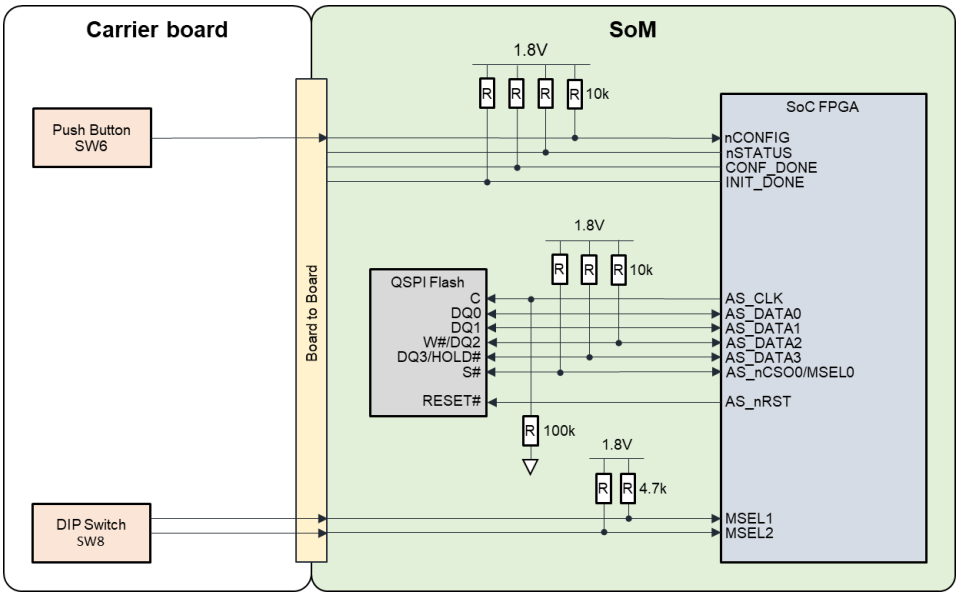


Figure 2-8 Configuration Circuit

2.6. **JTAG Connector**

The JTAG connector on this product can be used for evaluation and verification of the FPGA mounted on the SoM.

To use this function, connect an Altera FPGA Download Cable II or III to this connector.

For details on the specifications and usage of these cables, to the official Altera website.

The board layout, circuit, and pin assignments of this connector are shown below.

Figure 2-9 JTAG Connector Layout

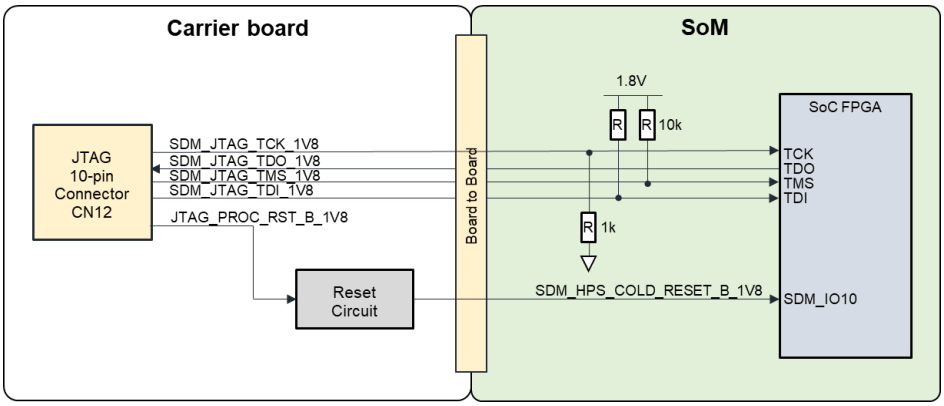


Figure 2-10 JTAG Circuit

Table 2-12 JTAG Circuit Pin Assignment

Pin No.	Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
1	SDM_JTAG_TCK_1V8	CN1.A58	SDM_JTAG_TCK_1V8	AF16	1.8-V LVCMOS
2	GND	N/A	N/A	N/A	N/A
3	SDM_JTAG_TDO_1V8	CN1.A60	SDM_JTAG_TDO_1V8	AE16	1.8-V LVCMOS
4	1.8V	N/A	N/A	N/A	N/A
5	SDM_JTAG_TMS_1V8	CN1.A57	SDM_JTAG_TMS_1V8	AF17	1.8-V LVCMOS
6	JTAG_PROC_RST_B_1V8	CN1.C58	SDM_HPS_COLD_RESET_B_1V8	AH11	1.8-V LVCMOS
7	N/A	N/A	N/A	N/A	N/A
8	N/A	N/A	N/A	N/A	N/A
9	SDM_JTAG_TDI_1V8	CN1.A59	SDM_JTAG_TDI_1V8	AE17	1.8-V LVCMOS
10	GND	N/A	N/A	N/A	N/A

2.7. **SDMMC**

This product is equipped with a microSD card slot on the carrier board, allowing a microSD card to be used as storage device. The SoM also includes onboard eMMC memory, which is mutually exclusive with the microSD card. The selection between them can be made using the SoM Mode Switch. For details on the SoM Mode Switch. For details on the SoM Mode Switch, refer to Selection 2.3.4.

The board layout, circuit, and pin assignments of the microSD card slot are shown below.

Figure 2-11 microSD Card Slot Layout

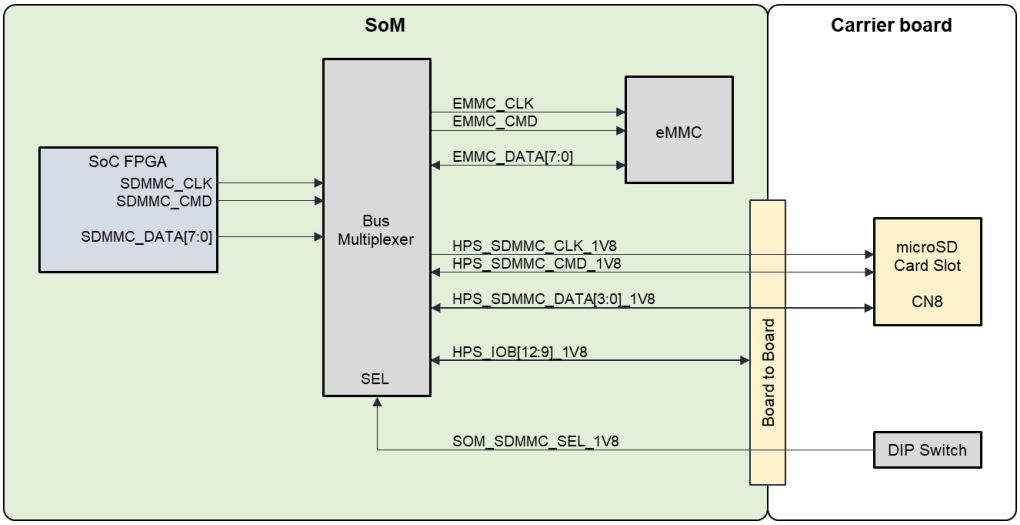


Figure 2-12 SDMMC Circuit

Table 2-13 SDMMC Circuit Pin Assignment

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
HPS_SDMMC_CLK_1V8	CN2.B7	HPS_SDMMC_CLK_1V8	A18	1.8-V LVCMOS
HPS_SDMMC_CMD_1V8	CN2.B6	HPS_SDMMC_CMD_1V8	E20	1.8-V LVCMOS
HPS_SDMMC_DATA0_1V8	CN2.B3	HPS_SDMMC_DATA0_1V8	D23	1.8-V LVCMOS
HPS_SDMMC_DATA1_1V8	CN2.B4	HPS_SDMMC_DATA1_1V8	C25	1.8-V LVCMOS
HPS_SDMMC_DATA2_1V8	CN2.B2	HPS_SDMMC_DATA2_1V8	C21	1.8-V LVCMOS
HPS_SDMMC_DATA3_1V8	CN2.B1	HPS_SDMMC_DATA3_1V8	C23	1.8-V LVCMOS
N/A*[1]	CN2.A3	HPS_IOB9_1V8	C22	1.8-V LVCMOS
N/A*[1]	CN2.A4	HPS_IOB10_1V8	D19	1.8-V LVCMOS
N/A*[1]	CN2.A5	HPS_IOB11_1V8	B21	1.8-V LVCMOS
N/A*[1]	CN2.A2	HPS_IOB12_1V8	A22	1.8-V LVCMOS
SOM_SDMMC_SEL_1V8	CN2.B56	SOM_SDMMC_SEL_1V8	N/A	1.8-V LVCMOS

*[1] These pins are assigned to the upper bits of the SDMMC data bus; therefore, they cannot be used as GPIO when the eMMC is operated in 8-bit mode. These pins are not connected on the carrier board.

2.8. **Reset Circuit**

The reset circuit of this product supports three reset sources: a power-on reset at power-up, reconfiguration via SW6, and an HPS cold reset via SW7. The layout, circuit, and pin assignments of the reset switches are shown below.

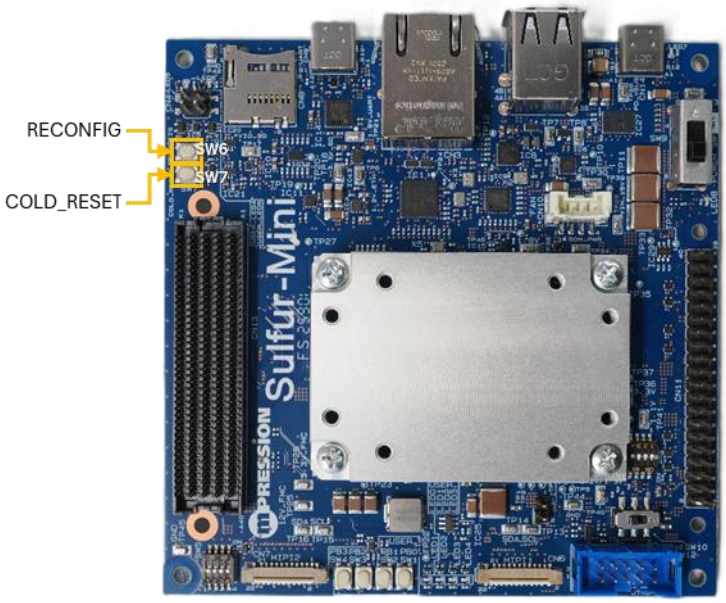


Figure 2-13 Reset Switch Layout

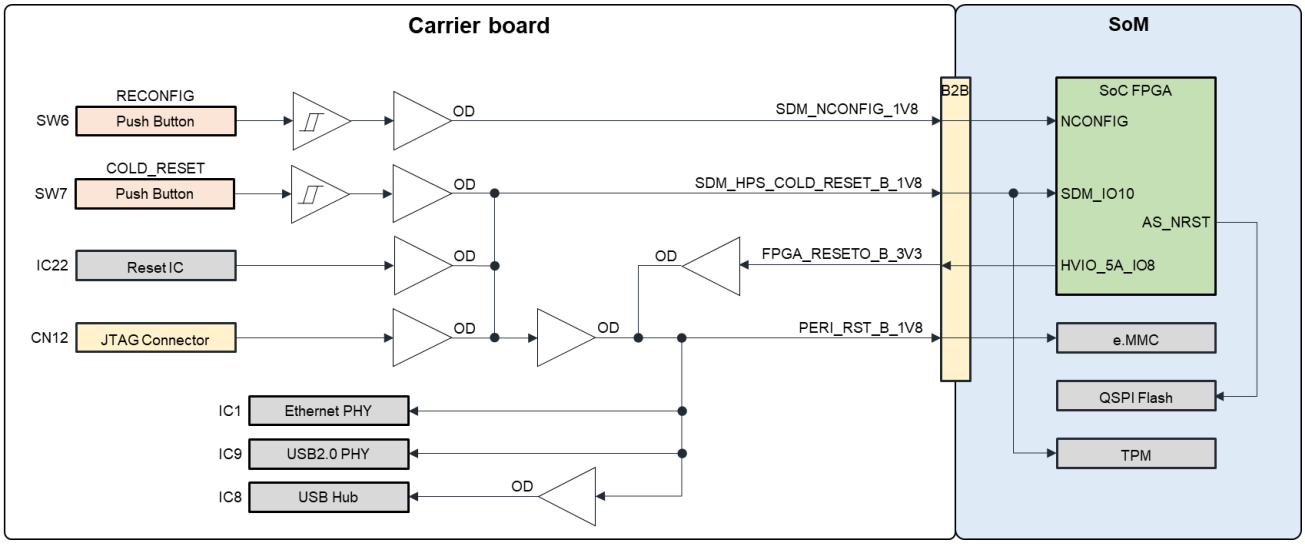


Figure 2-14 Reset Circuit

Table 2-14 Reset Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
SDM_NCONFIG_1V8	CN1.C59	SDM_NCONFIG_1V8	AG15	1.8-V LVCMOS
SDM_HPS_COLD_RESET_B_1V8	CN1.C58	SDM_HPS_COLD_RESET_B_1V8	AH11	1.8-V LVCMOS
FPGA_RESETO_B_3V3	CN2.A50	HVIO_5A_IO8	AH20	3.3-V LVCMOS
PERI_RST_B_1V8	CN2.B55	SOM_EMMC_RST_B_1V8	N/A	1.8-V LVCMOS

2.9. **Clock Circuit**

The clock circuit, and pin assignments of this product are shown below.

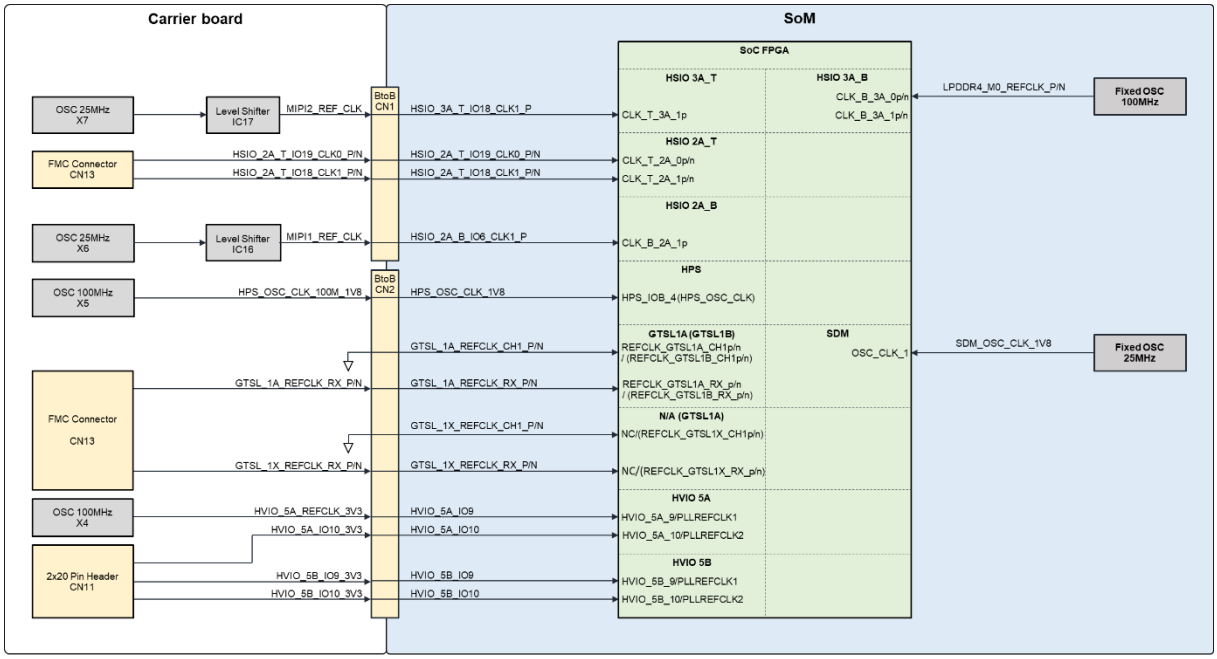


Figure 2-15 Clock Circuit

Table 2-15 Clock Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
HPS_OSC_CLK_100M_1V8	CN2.B14	HPS_OSC_CLK_1V8	C20	1.8-V LVCMOS
MIPI2_REF_CLK	CN1.A5	HSIO_3A_T_IO18_CLK1_P	F2	1.1-V
HSIO_2A_T_IO18_CLK1_P	CN1.B30	HSIO_2A_T_IO18_CLK1_P	AC6	1.3-V True Differential Signaling
HSIO_2A_T_IO18_CLK1_N	CN1.B29	HSIO_2A_T_IO18_CLK1_N	AC5	1.3-V True Differential Signaling
HSIO_2A_T_IO19_CLK0_P	CN1.D15	HSIO_2A_T_IO19_CLK0_P	N2	1.3-V True Differential Signaling
HSIO_2A_T_IO19_CLK0_N	CN1.D14	HSIO_2A_T_IO19_CLK0_N	N1	1.3-V True Differential Signaling
MIPI1_REF_CLK	CN1.A38	HSIO_2A_B_IO6_CLK1_P	AD5	1.2-V
GTSL_1A_REFCLK_RX_P	CN2.C28	GTSL_1A_REFCLK_RX_P	P25	Current Mode Logic (CML)
GTSL_1A_REFCLK_RX_N	CN2.C27	GTSL_1A_REFCLK_RX_N	P24	Current Mode Logic (CML)
GTSL_1X_REFCLK_RX_P	CN2.D38	GTSL_1X_REFCLK_RX_P	Y25*1	Current Mode Logic (CML)
GTSL_1X_REFCLK_RX_N	CN2.D37	GTSL_1X_REFCLK_RX_N	Y24*1	Current Mode Logic (CML)
HVIO_5A_REFCLK_3V3	CN2.A47	HVIO_5A_IO9	AJ22	3.3-V LVCMOS
HVIO_5A_IO10_3V3	CN2.A49	HVIO_5A_IO10	AJ20	3.3-V LVCMOS
HVIO_5B_IO9_3V3	CN2.D45	HVIO_5B_IO9	AJ27	3.3-V LVCMOS
HVIO_5B_IO10_3V3	CN2.C45	HVIO_5B_IO10	AH27	3.3-V LVCMOS

*1 These pins are not connected to the 013B device mounted on the SoM of this product. They are available only on the 028B device.

2.10. **Ethernet**

This product includes one Ethernet channel on the HPS side. The board layout, circuit, and pin assignments of the Ethernet connector are shown below.

Figure 2-16 Ethernet Connector Layout

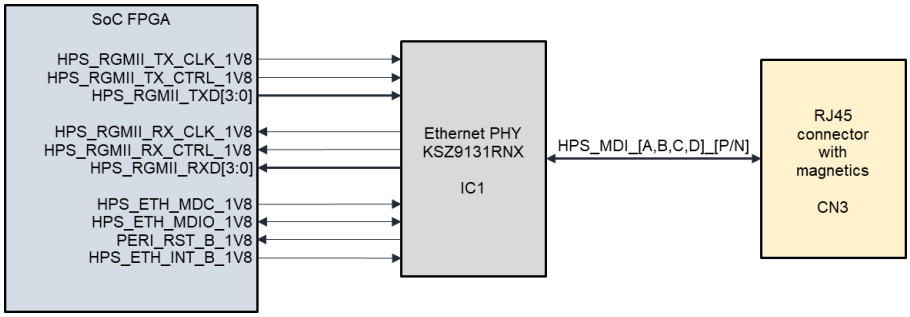


Figure 2-17 Ethernet Circuit

Table 2-16 Ethernet Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
HPS_RGMII_TX_CLK_1V8	CN2.C2	HPS_RGMII_TX_CLK_1V8	B16	1.8-V LVCMOS
HPS_RGMII_TX_CTRL_1V8	CN2.C3	HPS_RGMII_TX_CTRL_1V8	B18	1.8-V LVCMOS
HPS_RGMII_TXD0_1V8	CN2.C8	HPS_RGMII_TXD0_1V8	C18	1.8-V LVCMOS
HPS_RGMII_TXD1_1V8	CN2.C4	HPS_RGMII_TXD1_1V8	A21	1.8-V LVCMOS
HPS_RGMII_TXD2_1V8	CN2.C7	HPS_RGMII_TXD2_1V8	D18	1.8-V LVCMOS
HPS_RGMII_TXD3_1V8	CN2.C5	HPS_RGMII_TXD3_1V8	B19	1.8-V LVCMOS
HPS_RGMII_RX_CLK_1V8	CN2.D7	HPS_RGMII_RX_CLK_1V8	E19	1.8-V LVCMOS
HPS_RGMII_RX_CTRL_1V8	CN2.D6	HPS_RGMII_RX_CTRL_1V8	B20	1.8-V LVCMOS
HPS_RGMII_RXD0_1V8	CN2.D2	HPS_RGMII_RXD0_1V8	D17	1.8-V LVCMOS
HPS_RGMII_RXD1_1V8	CN2.D4	HPS_RGMII_RXD1_1V8	A19	1.8-V LVCMOS
HPS_RGMII_RXD2_1V8	CN2.D3	HPS_RGMII_RXD2_1V8	C17	1.8-V LVCMOS
HPS_RGMII_RXD3_1V8	CN2.D1	HPS_RGMII_RXD3_1V8	C16	1.8-V LVCMOS
HPS_ETH_MDC_1V8	CN2.C10	HPS_ETH_MDC_1V8	E22	1.8-V LVCMOS

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
HPS_ETH_MDIO_1V8	CN2.C9	HPS_ETH_MDIO_1V8	D27	1.8-V LVCMOS
HPS_ETH_INT_B_1V8	CN2.C12	HPS_ETH_INT_B_1V8	A27	1.8-V LVCMOS

2.11. **1PPS Connector**

The 1PPS connector is used for input and output of TSN synchronization signals. The circuit and pin assignments are shown below.

Figure 2-18 1PPS Connector Layout

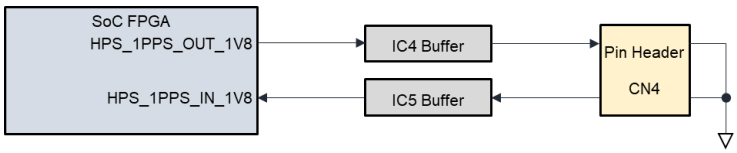


Figure 2-19 1PPS Circuit

Table 2-17 1PPS Circuit Pin Assignments

Pin No.	Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
1	HPS_1PPS_OUT_1V8	CN2.D14	HPS_1PPS_OUT_1V8	B28	1.8-V LVCMOS
2	GND	N/A	N/A	N/A	N/A
3	HPS_1PPS_IN_1V8	CN2.D13	HPS_1PPS_IN_1V8	F23	1.8-V LVCMOS
4	GND	N/A	N/A	N/A	N/A

2.12. **USB2.0**

This product provides two USB 2.0 host ports (USB Type-A). These ports are expanded from the HPS USB interface using an onboard single transaction translator (STT) hub. The board layout, circuit, and pin assignments of the USB 2.0 connectors are shown below.

Figure 2-20 USB 2.0 Connector Layout

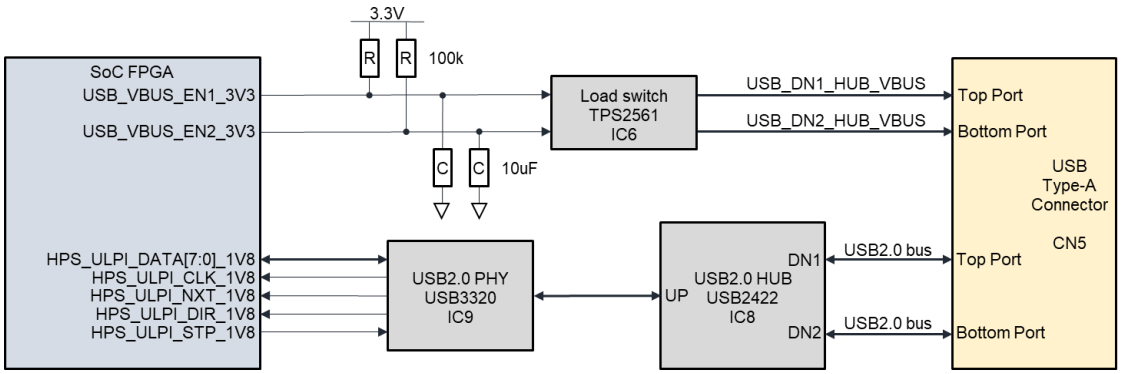


Figure 2-21 USB 2.0 Circuit

Table 2-18 USB 2.0 Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
USB_VBUS_EN1_3V3	CN2.B45	HVIO_5A_IO2	AJ23	3.3-V LVCMOS
USB_VBUS_EN2_3V3	CN2.B48	HVIO_5A_IO3	AH21	3.3-V LVCMOS
HPS_ULPI_CLK_1V8	CN2.B13	HPS_ULPI_CLK_1V8	D25	1.8-V LVCMOS
HPS_ULPI_DATA0_1V8	CN2.B8	HPS_ULPI_DATA0_1V8	E17	1.8-V LVCMOS
HPS_ULPI_DATA1_1V8	CN2.B9	HPS_ULPI_DATA1_1V8	A16	1.8-V LVCMOS
HPS_ULPI_DATA2_1V8	CN2.B11	HPS_ULPI_DATA2_1V8	D24	1.8-V LVCMOS
HPS_ULPI_DATA3_1V8	CN2.A10	HPS_ULPI_DATA3_1V8	E21	1.8-V LVCMOS
HPS_ULPI_DATA4_1V8	CN2.B12	HPS_ULPI_DATA4_1V8	B23	1.8-V LVCMOS
HPS_ULPI_DATA5_1V8	CN2.A9	HPS_ULPI_DATA5_1V8	D20	1.8-V LVCMOS
HPS_ULPI_DATA6_1V8	CN2.A13	HPS_ULPI_DATA6_1V8	B24	1.8-V LVCMOS

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
HPS_ULPI_DATA7_1V8	CN2.A12	HPS_ULPI_DATA7_1V8	A24	1.8-V LVCMOS
HPS_ULPI_DIR_1V8	CN2.A15	HPS_ULPI_DIR_1V8	B25	1.8-V LVCMOS
HPS_ULPI_NXT_1V8	CN2.A8	HPS_ULPI_NXT_1V8	E16	1.8-V LVCMOS
HPS_ULPI_STP_1V8	CN2.A14	HPS_ULPI_STP_1V8	B26	1.8-V LVCMOS

2.13. **USB-UART**

The board layout, circuit, and pin assignments of the USB-UART connector (USB-Type-C) of this product are shown below.

Figure 2-22 USB-UART Connector Layout

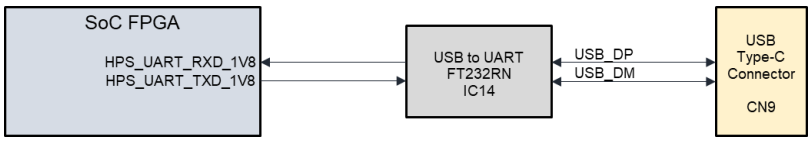


Figure 2-23 USB-UART Circuit

Table 2-19 USB-UART Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
HPS_UART_TXD_1V8	CN2.C15	HPS_UART_TXD_1V8	C27	1.8-V LVCMOS
HPS_UART_RXD_1V8	CN2.C14	HPS_UART_RXD_1V8	F24	1.8-V LVCMOS

2.14. **MIPI**

The board layout, circuit, and pin assignments of the MIPI connector are shown below. When using MIPI, set SW10 (HSIO_2A Voltage Select Switch) to 1.2 V position. For details on the HSIO_2A Voltage Select Switch, refer to Selection2.3.5.

Figure 2-24 MIPI Connector Layout

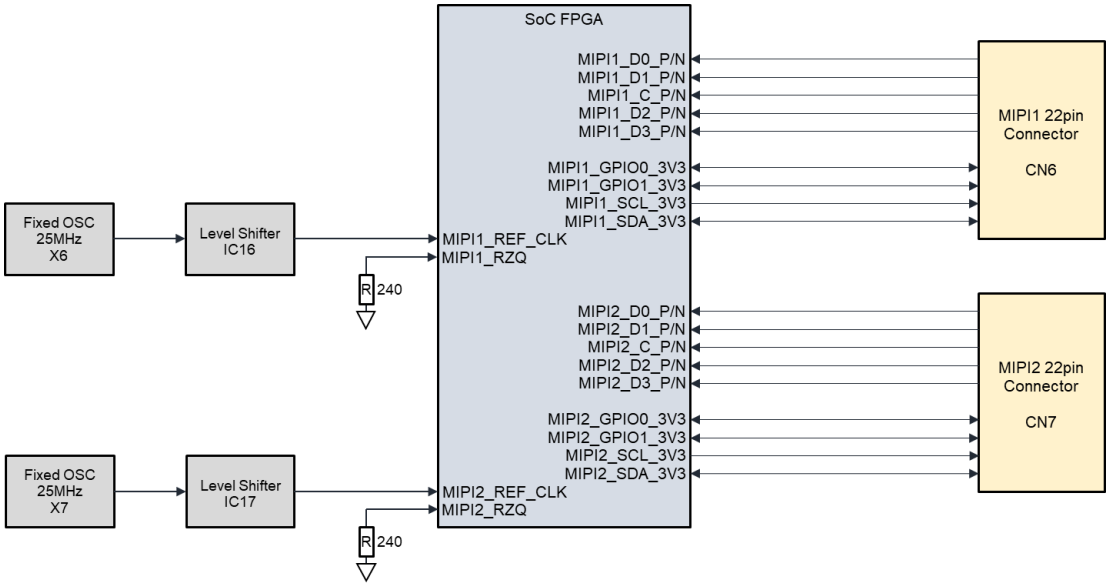


Figure 2-25 MIPI Circuit

Table 2-20 MIPI Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
MIPI1_REF_CLK	CN1.A38	HSIO_2A_B_IO6_CLK1_P	AD5	1.2-V
MIPI1_RZQ	CN1.B39	HSIO_2A_B_IO5_P	AD3	1.2-V
MIPI1_D0_N	CN1.A49	HSIO_2A_B_IO12_N	AE7	DPHY
MIPI1_D0_P	CN1.A50	HSIO_2A_B_IO12_P	AF7	DPHY
MIPI1_D1_N	CN1.A46	HSIO_2A_B_IO11_N	AE6	DPHY
MIPI1_D1_P	CN1.A47	HSIO_2A_B_IO11_P	AF6	DPHY
MIPI1_C_N	CN1.B47	HSIO_2A_B_IO10_N	AG5	DPHY
MIPI1_C_P	CN1.B48	HSIO_2A_B_IO10_P	AH5	DPHY
MIPI1_D2_N	CN1.B50	HSIO_2A_B_IO9_N	AG6	DPHY
MIPI1_D2_P	CN1.B51	HSIO_2A_B_IO9_P	AH6	DPHY
MIPI1_D3_N	CN1.A43	HSIO_2A_B_IO8_N	AG4	DPHY
MIPI1_D3_P	CN1.A44	HSIO_2A_B_IO8_P	AF4	DPHY
MIPI1_GPIO0_3V3	CN2.B52	HVIO_5A_IO20	AF21	3.3-V LVCMOS
MIPI1_GPIO1_3V3	CN2.B53	HVIO_5A_IO19	AF19	3.3-V LVCMOS
MIPI1_SCL_3V3	CN2.B43	HVIO_5A_IO18	AF22	3.3-V LVCMOS
MIPI1_SDA_3V3	CN2.A52	HVIO_5A_IO17	AG19	3.3-V LVCMOS
MIPI2_REF_CLK	CN1.A5	HSIO_3A_T_IO18_CLK1_P	F2	1.1-V
MIPI2_RZQ	CN1.A8	HSIO_3A_T_IO17_P	G1	1.1-V
MIPI2_D0_N	CN1.C1	HSIO_3A_T_IO24_N	D4	DPHY
MIPI2_D0_P	CN1.C2	HSIO_3A_T_IO24_P	C5	DPHY
MIPI2_D1_N	CN1.B2	HSIO_3A_T_IO23_N	E6	DPHY
MIPI2_D1_P	CN1.B3	HSIO_3A_T_IO23_P	F6	DPHY
MIPI2_C_N	CN1.A1	HSIO_3A_T_IO22_N	E5	DPHY
MIPI2_C_P	CN1.A2	HSIO_3A_T_IO22_P	D5	DPHY
MIPI2_D2_N	CN1.B5	HSIO_3A_T_IO21_N	E4	DPHY
MIPI2_D2_P	CN1.B6	HSIO_3A_T_IO21_P	F4	DPHY
MIPI2_D3_N	CN1.B8	HSIO_3A_T_IO20_N	F3	DPHY
MIPI2_D3_P	CN1.B9	HSIO_3A_T_IO20_P	G3	DPHY
MIPI2_GPIO0_3V3	CN2.B50	HVIO_5A_IO16	AG20	3.3-V LVCMOS
MIPI2_GPIO1_3V3	CN2.A41	HVIO_5A_IO15	AF23	3.3-V LVCMOS
MIPI2_SCL_3V3	CN2.B42	HVIO_5A_IO14	AG24	3.3-V LVCMOS
MIPI2_SDA_3V3	CN2.A42	HVIO_5A_IO13	AF24	3.3-V LVCMOS

2.15. I2C Circuit

The circuit and pin assignments of the I2C interface are shown below.

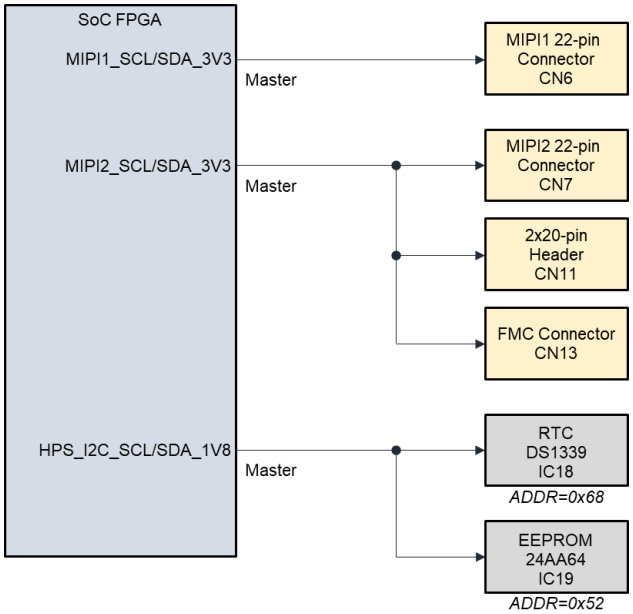


Figure 2-26 I2C Circuit

Table 2-21 I2C Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
MIPI1_SCL_3V3	CN2.B43	HVIO_5A_IO18	AF22	3.3-V LVCMOS
MIPI1_SDA_3V3	CN2.A52	HVIO_5A_IO17	AG19	3.3-V LVCMOS
MIPI2_SCL_3V3	CN2.B42	HVIO_5A_IO14	AG24	3.3-V LVCMOS
MIPI2_SDA_3V3	CN2.A42	HVIO_5A_IO13	AF24	3.3-V LVCMOS
HPS_I2C_SCL_1V8	CN2.D8	HPS_I2C_SCL_1V8	D22	1.8-V
HPS_I2C_SDA_1V8	CN2.D9	HPS_I2C_SDA_1V8	C26	1.8-V

2.16. **FAN Power Connector**

This product does not include a fan; however, a FAN power connector is provided for evaluation purposes.

The board layout, circuit and pin assignments of the FAN power connector are shown below.

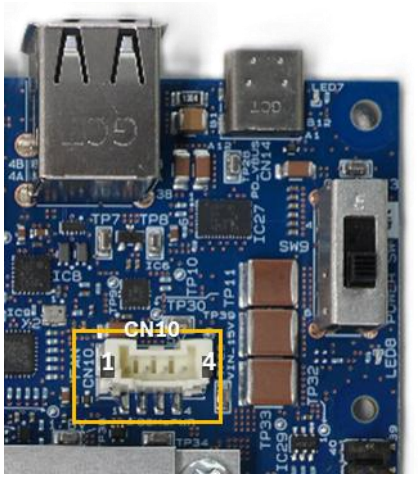


Figure 2-27 FAN Power Connector

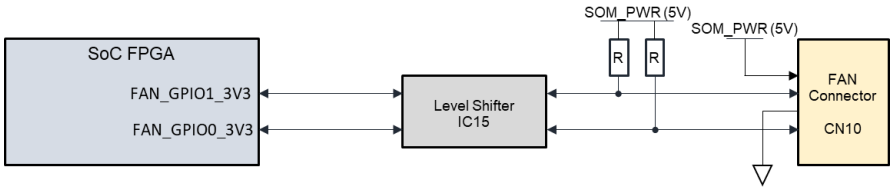


Figure 2-28 FAN Power Connector Circuit

Table 2-22 FAN Power Connector Circuit Pin Assignments

Pin No.	Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	I/O Standard
1	FAN Power (5V)	N/A	N/A	N/A	N/A
2	FAN_GPIO1_3V3*1	CN2.B46	HVIO_5A_IO1	AJ24	3.3-V LVCMOS
3	GND	N/A	N/A	N/A	N/A
4	FAN_GPIO0_3V3*1	CN2.A44	HVIO_5A_IO7	AG23	3.3-V LVCMOS

*1 These pins can be used as required, for example for fan speed control and monitoring, depending on the application.

2.17. **2 x 20 Pin Header**

The board layout and pin assignments of the 2 x 20 pin header are shown below.

Figure 2-29 2 x 20 Pin Header Layout

Table 2-23 2 x20 Pin Header Pin Assignments

Pin No.	Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	Description
1	3.3V	N/A	N/A	N/A	3.3V output
2	5V_LS	N/A	N/A	N/A	5V output
3	MIPI2_SCL_3V3	CN2.B42	HVIO_5A_IO14	AG24	3.3-V LVCMOS
4	5V_LS	N/A	N/A	N/A	5V output
5	MIPI2_SDA_3V3	CN2.A42	HVIO_5A_IO13	AF24	3.3-V LVCMOS
6	GND	N/A	N/A	N/A	Ground
7	HVIO_5B_IO1_3V3	CN2.D48	HVIO_5B_IO1	AK24	3.3-V LVCMOS
8	HVIO_5B_IO2_3V3	CN2.C47	HVIO_5B_IO2	AH26	3.3-V LVCMOS
9	GND	N/A	N/A	N/A	Ground
10	HVIO_5B_IO3_3V3	CN2.D47	HVIO_5B_IO3	AJ25	3.3-V LVCMOS
11	HVIO_5B_IO4_3V3	CN2.C50	HVIO_5B_IO4	AH25	3.3-V LVCMOS
12	HVIO_5B_IO5_3V3	CN2.C49	HVIO_5B_IO5	AG26	3.3-V LVCMOS
13	HVIO_5B_IO6_3V3	CN2.C51	HVIO_5B_IO6	AE25	3.3-V LVCMOS
14	GND	N/A	N/A	N/A	Ground
15	HVIO_5B_IO7_3V3	CN2.C46	HVIO_5B_IO7	AK25	3.3-V LVCMOS
16	HVIO_5B_IO8_3V3	CN2.D51	HVIO_5B_IO8	AF26	3.3-V LVCMOS
17	3.3V	N/A	N/A	N/A	3.3V output
18	HVIO_5B_IO9_3V3	CN2.D45	HVIO_5B_IO9	AJ27	3.3-V LVCMOS
19	HVIO_5B_IO10_3V3	CN2.C45	HVIO_5B_IO10	AH27	3.3-V LVCMOS
20	GND	N/A	N/A	N/A	Ground
21	HVIO_5B_IO11_3V3	CN2.D53	HVIO_5B_IO11	AK19	3.3-V LVCMOS
22	HVIO_5B_IO12_3V3	CN2.D50	HVIO_5B_IO12	AK22	3.3-V LVCMOS
23	HVIO_5B_IO13_3V3	CN2.D42	HVIO_5B_IO13	AJ29	3.3-V LVCMOS
24	HVIO_5B_IO15_3V3	CN2.C41	HVIO_5B_IO15	AH28	3.3-V LVCMOS
25	GND	N/A	N/A	N/A	Ground
26	HVIO_5B_IO14_3V3	CN2.D46	HVIO_5B_IO14	AK26	3.3-V LVCMOS
27	N/A	N/A	N/A	N/A	3.3-V LVCMOS
28	N/A	N/A	N/A	N/A	3.3-V LVCMOS
29	HVIO_5A_IO5_3V3	CN2.A45	HVIO_5A_IO5	AH23	3.3-V LVCMOS
30	GND	N/A	N/A	N/A	Ground

Pin No.	Signal Name	BtoB Pin	SoM Pin Name	FPGA Pin	Description
31	HVIO_5A_IO6_3V3	CN2.A46	HVIO_5A_IO6	AH22	3.3-V LVCMOS
32	HVIO_5B_IO16_3V3	CN2.D52	HVIO_5B_IO16	AK20	3.3-V LVCMOS
33	HVIO_5B_IO17_3V3	CN2.C42	HVIO_5B_IO17	AF27	3.3-V LVCMOS
34	GND	N/A	N/A	N/A	Ground
35	HVIO_5B_IO18_3V3	CN2.D43	HVIO_5B_IO18	AJ28	3.3-V LVCMOS
36	HVIO_5A_IO10_3V3	CN2.A49	HVIO_5A_IO10	AJ20	3.3-V LVCMOS
37	HVIO_5A_IO4_3V3	CN2.B51	HVIO_5A_IO4	AJ19	3.3-V LVCMOS
38	HVIO_5B_IO19_3V3	CN2.C52	HVIO_5B_IO19	AK21	3.3-V LVCMOS
39	GND	N/A	N/A	N/A	Ground
40	HVIO_5B_IO20_3V3	CN2.C44	HVIO_5B_IO20	AK27	3.3-V LVCMOS

2.18. **FMC Connector**

This product is equipped with a 400-pin FMC connector of a VITA™ 57.1 FMC HPC module. The board layout and pin mapping of the FMC connector are shown below.

Figure 2-30 FMC Connector Layout

Pin No.	K	J	H	G	F	E	D	C	B	A
1	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	*CLK_DIR*	GND
2	GND	NC	PRSNT_M2C_L	CLK1_M2C_P	GND	NC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	NC	GND	CLK1_M2C_N	GND	NC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	NC	GND	CLK0_M2C_P	GND	NC	GND	GBTCLK0_M2C_P	GND	NC	GND
5	NC	GND	CLK0_M2C_N	GND	NC	GND	GBTCLK0_M2C_N	GND	NC	GND
6	GND	NC	GND	LA00_P_CC	GND	NC	GND	DP0_M2C_P	GND	DP2_M2C_P
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	GND	DP2_M2C_N
8	NC	GND	LA02_N	GND	NC	GND	LA01_P_CC	GND	NC	GND
9	GND	NC	GND	LA03_P	GND	NC	LA01_N_CC	GND	NC	GND
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	GND	DP3_M2C_P
11	NC	GND	LA04_N	GND	NC	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	NC	GND	LA08_P	GND	NC	LA05_N	GND	DP7_M2C_P	GND
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	DP7_M2C_N	GND
14	NC	GND	LA07_N	GND	NC	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	NC	GND	LA12_P	GND	NC	LA09_N	LA10_N	GND	DP4_M2C_N
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	DP6_M2C_P	GND
17	NC	GND	LA11_N	GND	NC	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	NC	GND	LA16_P	GND	NC	LA13_N	LA14_P	GND	DP5_M2C_P
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	GND	DP5_M2C_N
20	NC	GND	LA15_N	GND	NC	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	NC	GND	LA20_P	GND	NC	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	GND	DP1_C2M_P
23	NC	GND	LA19_N	GND	NC	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	NC	GND	LA22_P	GND	NC	LA23_N	GND	NC	GND
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	GND
26	NC	GND	LA21_N	GND	NC	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	NC	GND	LA25_P	GND	NC	LA26_N	LA27_N	GND	DP2_C2M_N
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	GND
29	NC	GND	LA24_N	GND	NC	GND	NC	GND	NC	GND
30	GND	NC	GND	LA29_P	GND	NC	NC	SCL	GND	DP3_C2M_P
31	NC	NC	LA28_P	LA29_N	NC	NC	NC	SDA	GND	DP3_C2M_N
32	NC	GND	LA28_N	GND	NC	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	NC	GND	LA31_P	GND	NC	NC	GND	DP7_C2M_N	GND
34	NC	NC	LA30_P	LA31_N	NC	NC	NC	GA0	GND	DP4_C2M_P
35	NC	GND	LA30_N	GND	NC	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	NC	GND	LA33_P	GND	NC	3P3V	GND	DP6_C2M_P	GND
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	DP6_C2M_N	GND
38	NC	GND	LA32_N	GND	NC	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	NC	GND

Figure 2-31 FMC Connector Pin Mapping

Connector Part Number : ASP-134486-01 (Samtec)

Mating Connector (Stack Height: 8.5mm) : ASP-134602-01 (Samtec)

Mating Connector (Stack Height: 10mm) : ASP-134488-01 (Samtec)

2.18.1. **FMC Connector Signal Names and Description**

Table 2-24 2.18.1. FMC Connector Signal Names and Description

Pin No.	FMC Vita 57.1	Carrier Board Signal Name	SoM Pin Name	FPGA Pin Name	FPGA Pin	FPGA IO	Description
A1	GND	GND	GND	GND	GND	Power	Ground
A2	DP1_M2C_P	GTSL_1A_RX_CH1_P	GTSL_1A_RX_CH1_P	GTSL1A_RX_CH1P	H30	Input	Transceiver Bank 1A RX Channel 1 (P)
A3	DP1_M2C_N	GTSL_1A_RX_CH1_N	GTSL_1A_RX_CH1_N	GTSL1A_RX_CH1N	H29	Input	Transceiver Bank 1A RX Channel 1 (N)
A4	GND	GND	GND	GND	GND	Power	Ground
A5	GND	GND	GND	GND	GND	Power	Ground
A6	DP2_M2C_P	GTSL_1A_RX_CH2_P	GTSL_1A_RX_CH2_P	GTSL1A_RX_CH2P	F30	Input	Transceiver Bank 1A RX Channel 2 (P)
A7	DP2_M2C_N	GTSL_1A_RX_CH2_N	GTSL_1A_RX_CH2_N	GTSL1A_RX_CH2N	F29	Input	Transceiver Bank 1A RX Channel 2 (N)
A8	GND	GND	GND	GND	GND	Power	Ground
A9	GND	GND	GND	GND	GND	Power	Ground
A10	DP3_M2C_P	GTSL_1A_RX_CH3_P	GTSL_1A_RX_CH3_P	GTSL1A_RX_CH3P	D30	Input	Transceiver Bank 1A RX Channel 3 (P)
A11	DP3_M2C_N	GTSL_1A_RX_CH3_N	GTSL_1A_RX_CH3_N	GTSL1A_RX_CH3N	D29	Input	Transceiver Bank 1A RX Channel 3 (N)
A12	GND	GND	GND	GND	GND	Power	Ground
A13	GND	GND	GND	GND	GND	Power	Ground
A14	DP4_M2C_P	GTSL_1X_RX_CH0_P	GTSL_1X_RX_CH0_P	N/A	N/A	N/A	Not connected (028B variant only)
A15	DP4_M2C_N	GTSL_1X_RX_CH0_N	GTSL_1X_RX_CH0_N	N/A	N/A	N/A	Not connected (028B variant only)
A16	GND	GND	GND	GND	GND	Power	Ground
A17	GND	GND	GND	GND	GND	Power	Ground
A18	DP5_M2C_P	GTSL_1X_RX_CH1_P	GTSL_1X_RX_CH1_P	N/A	N/A	N/A	Not connected (028B variant only)
A19	DP5_M2C_N	GTSL_1X_RX_CH1_N	GTSL_1X_RX_CH1_N	N/A	N/A	N/A	Not connected (028B variant only)
A20	GND	GND	GND	GND	GND	Power	Ground
A21	GND	GND	GND	GND	GND	Power	Ground
A22	DP1_C2M_P	GTSL_1A_TX_CH1_P	GTSL_1A_TX_CH1_P	GTSL1A_TX_CH1P	M29	Output	Transceiver Bank 1A TX Channel 1 (P)
A23	DP1_C2M_N	GTSL_1A_TX_CH1_N	GTSL_1A_TX_CH1_N	GTSL1A_TX_CH1N	M28	Output	Transceiver Bank 1A TX Channel 1 (N)
A24	GND	GND	GND	GND	GND	Power	Ground
A25	GND	GND	GND	GND	GND	Power	Ground
A26	DP2_C2M_P	GTSL_1A_TX_CH2_P	GTSL_1A_TX_CH2_P	GTSL1A_TX_CH2P	K27	Output	Transceiver Bank 1A TX Channel 2 (P)
A27	DP2_C2M_N	GTSL_1A_TX_CH2_N	GTSL_1A_TX_CH2_N	GTSL1A_TX_CH2N	J27	Output	Transceiver Bank 1A TX Channel 2 (N)
A28	GND	GND	GND	GND	GND	Power	Ground
A29	GND	GND	GND	GND	GND	Power	Ground
A30	DP3_C2M_P	GTSL_1A_TX_CH3_P	GTSL_1A_TX_CH3_P	GTSL1A_TX_CH3P	G27	Output	Transceiver Bank 1A TX Channel 3 (P)
A31	DP3_C2M_N	GTSL_1A_TX_CH3_N	GTSL_1A_TX_CH3_N	GTSL1A_TX_CH3N	F27	Output	Transceiver Bank 1A TX Channel 3 (N)
A32	GND	GND	GND	GND	GND	Power	Ground
A33	GND	GND	GND	GND	GND	Power	Ground
A34	DP4_C2M_P	GTSL_1X_TX_CH0_P	GTSL_1X_TX_CH0_P	N/A	N/A	N/A	Not connected (028B variant only)
A35	DP4_C2M_N	GTSL_1X_TX_CH0_N	GTSL_1X_TX_CH0_N	N/A	N/A	N/A	Not connected (028B variant only)
A36	GND	GND	GND	GND	GND	Power	Ground
A37	GND	GND	GND	GND	GND	Power	Ground
A38	DP5_C2M_P	GTSL_1X_TX_CH1_P	GTSL_1X_TX_CH1_P	N/A	N/A	N/A	Not connected (028B variant only)
A39	DP5_C2M_N	GTSL_1X_TX_CH1_N	GTSL_1X_TX_CH1_N	N/A	N/A	N/A	Not connected (028B variant only)
A40	GND	GND	GND	GND	GND	Power	Ground
B1	CLK_DIR	GND	N/A	N/A	N/A	N/A	Direction signal for FMC CLK[2:3] (not used; tied to GND)
B2	GND	GND	GND	GND	GND	Power	Ground

Pin No.	FMC Vita 57.1	Carrier Board Signal Name	SoM Pin Name	FPGA Pin Name	FPGA Pin	FPGA IO	Description
B3	GND	GND	GND	GND	GND	Power	Ground
B4	DP9_M2C_P	N/A	N/A	N/A	N/A	N/A	Not connected
B5	DP9_M2C_N	N/A	N/A	N/A	N/A	N/A	Not connected
B6	GND	GND	GND	GND	GND	Power	Ground
B7	GND	GND	GND	GND	GND	Power	Ground
B8	DP8_M2C_P	N/A	N/A	N/A	N/A	N/A	Not connected
B9	DP8_M2C_N	N/A	N/A	N/A	N/A	N/A	Not connected
B10	GND	GND	GND	GND	GND	Power	Ground
B11	GND	GND	GND	GND	GND	Power	Ground
B12	DP7_M2C_P	GTSL_1X_RX_CH3_P	GTSL_1X_RX_CH3_P	N/A	N/A	N/A	Not connected (028B variant only)
B13	DP7_M2C_N	GTSL_1X_RX_CH3_N	GTSL_1X_RX_CH3_N	N/A	N/A	N/A	Not connected (028B variant only)
B14	GND	GND	GND	GND	GND	Power	Ground
B15	GND	GND	GND	GND	GND	Power	Ground
B16	DP6_M2C_P	GTSL_1X_RX_CH2_P	GTSL_1X_RX_CH2_P	N/A	N/A	N/A	Not connected (028B variant only)
B17	DP6_M2C_N	GTSL_1X_RX_CH2_N	GTSL_1X_RX_CH2_N	N/A	N/A	N/A	Not connected (028B variant only)
B18	GND	GND	GND	GND	GND	Power	Ground
B19	GND	GND	GND	GND	GND	Power	Ground
B20	GBTCLK1_M2C_P	GTSL_1X_REFCLK_RX_P	GTSL_1X_REFCLK_RX_P	N/A	N/A	N/A	Not connected (028B variant only)
B21	GBTCLK1_M2C_N	GTSL_1X_REFCLK_RX_N	GTSL_1X_REFCLK_RX_N	N/A	N/A	N/A	Not connected (028B variant only)
B22	GND	GND	GND	GND	GND	Power	Ground
B23	GND	GND	GND	GND	GND	Power	Ground
B24	DP9_C2M_P	N/A	N/A	N/A	N/A	N/A	Not connected
B25	DP9_C2M_N	N/A	N/A	N/A	N/A	N/A	Not connected
B26	GND	GND	GND	GND	GND	Power	Ground
B27	GND	GND	GND	GND	GND	Power	Ground
B28	DP8_C2M_P	N/A	N/A	N/A	N/A	N/A	Not connected
B29	DP8_C2M_N	N/A	N/A	N/A	N/A	N/A	Not connected
B30	GND	GND	GND	GND	GND	Power	Ground
B31	GND	GND	GND	GND	GND	Power	Ground
B32	DP7_C2M_P	GTSL_1X_TX_CH3_P	GTSL_1X_TX_CH3_P	N/A	N/A	N/A	Not connected (028B variant only)
B33	DP7_C2M_N	GTSL_1X_TX_CH3_N	GTSL_1X_TX_CH3_N	N/A	N/A	N/A	Not connected (028B variant only)
B34	GND	GND	GND	GND	GND	Power	Ground
B35	GND	GND	GND	GND	GND	Power	Ground
B36	DP6_C2M_P	GTSL_1X_TX_CH2_P	GTSL_1X_TX_CH2_P	N/A	N/A	N/A	Not connected (028B variant only)
B37	DP6_C2M_N	GTSL_1X_TX_CH2_N	GTSL_1X_TX_CH2_N	N/A	N/A	N/A	Not connected (028B variant only)
B38	GND	GND	GND	GND	GND	Power	Ground
B39	GND	GND	GND	GND	GND	Power	Ground
B40	RES0	N/A	N/A	N/A	N/A	N/A	Not connected
C1	GND	GND	GND	GND	GND	Power	Ground
C2	DP0_C2M_P	GTSL_1A_TX_CH0_P	GTSL_1A_TX_CH0_P	GTSL1A_TX_CH0P	P30	Output	Transceiver Bank 1A TX Channel 0 (P)
C3	DP0_C2M_N	GTSL_1A_TX_CH0_N	GTSL_1A_TX_CH0_N	GTSL1A_TX_CH0N	P29	Output	Transceiver Bank 1A TX Channel 0 (N)
C4	GND	GND	GND	GND	GND	Power	Ground
C5	GND	GND	GND	GND	GND	Power	Ground
C6	DP0_M2C_P	GTSL_1A_RX_CH0_P	GTSL_1A_RX_CH0_P	GTSL1A_RX_CH0P	K30	Input	Transceiver Bank 1A RX Channel 0 (P)
C7	DP0_M2C_N	GTSL_1A_RX_CH0_N	GTSL_1A_RX_CH0_N	GTSL1A_RX_CH0N	K29	Input	Transceiver Bank 1A RX Channel 0 (N)
C8	GND	GND	GND	GND	GND	Power	Ground
C9	GND	GND	GND	GND	GND	Power	Ground

Pin No.	FMC Vita 57.1	Carrier Board Signal Name	SoM Pin Name	FPGA Pin Name	FPGA Pin	FPGA IO	Description
C10	LA06_P	HSIO_2A_B_IO18_P	HSIO_2A_B_IO18_P	IOB,DIFF_IO_2A_B18P	AB1	I/O	HSIO Bank 2A_B IO18 differential (P) / single-ended
C11	LA06_N	HSIO_2A_B_IO18_N	HSIO_2A_B_IO18_N	IOB,DIFF_IO_2A_B18N	AA2	I/O	HSIO Bank 2A_B IO18 differential (N) / single-ended
C12	GND	GND	GND	GND	GND	Power	Ground
C13	GND	GND	GND	GND	GND	Power	Ground
C14	LA10_P	HSIO_2A_T_IO11_P	HSIO_2A_T_IO11_P	IOB,DIFF_IO_2A_T11P	U4	I/O	HSIO Bank 2A_T IO11 differential (P) / single-ended
C15	LA10_N	HSIO_2A_T_IO11_N	HSIO_2A_T_IO11_N	IOB,DIFF_IO_2A_T11N	U3	I/O	HSIO Bank 2A_T IO11 differential (N) / single-ended
C16	GND	GND	GND	GND	GND	Power	Ground
C17	GND	GND	GND	GND	GND	Power	Ground
C18	LA14_P	HSIO_2A_T_IO22_P	HSIO_2A_T_IO22_P	IOB,DIFF_IO_2A_T22P	T2	I/O	HSIO Bank 2A_T IO22 differential (P) / single-ended
C19	LA14_N	HSIO_2A_T_IO22_N	HSIO_2A_T_IO22_N	IOB,DIFF_IO_2A_T22N	U1	I/O	HSIO Bank 2A_T IO22 differential (N) / single-ended
C20	GND	GND	GND	GND	GND	Power	Ground
C21	GND	GND	GND	GND	GND	Power	Ground
C22	LA18_P_CC	HSIO_2A_T_IO21_P	HSIO_2A_T_IO21_P	IOB,DIFF_IO_2A_T21P	R2	I/O	HSIO Bank 2A_T IO21 differential (P) / single-ended
C23	LA18_N_CC	HSIO_2A_T_IO21_N	HSIO_2A_T_IO21_N	IOB,DIFF_IO_2A_T21N	T1	I/O	HSIO Bank 2A_T IO21 differential (N) / single-ended
C24	GND	GND	GND	GND	GND	Power	Ground
C25	GND	GND	GND	GND	GND	Power	Ground
C26	LA27_P	HSIO_2A_T_IO4_P	HSIO_2A_T_IO4_P	IOB,DIFF_IO_2A_T4P	R5	I/O	HSIO Bank 2A_T IO4 differential (P) / single-ended
C27	LA27_N	HSIO_2A_T_IO4_N	HSIO_2A_T_IO4_N	IOB,DIFF_IO_2A_T4N	R6	I/O	HSIO Bank 2A_T IO4 differential (N) / single-ended
C28	GND	GND	GND	GND	GND	Power	Ground
C29	GND	GND	GND	GND	GND	Power	Ground
C30	SCL	FMC_I2C_SCL_3V3	HVIO_5A_IO14	HVIO_5A_IO14	AG24	Output, 3.3V	FMC I2C clock (SCL)
C31	SDA	FMC_I2C_SDA_3V3	HVIO_5A_IO13	HVIO_5A_IO13	AF24	I/O, 3.3V	FMC I2C data (SDA)
C32	GND	GND	GND	GND	GND	Power	Ground
C33	GND	GND	GND	GND	GND	Power	Ground
C34	GA0	FMC_GA0	N/A	N/A	N/A	N/A	FMC GA0 signal (pulled down on the carrier board)
C35	12P0V	12V_FMC	N/A	N/A	N/A	N/A	FMC 12 V power input (supplied from the carrier board)
C36	GND	GND	GND	GND	GND	Power	Ground
C37	12P0V	12V_FMC	N/A	N/A	N/A	N/A	FMC 12 V power input (supplied from the carrier board)
C38	GND	GND	GND	GND	GND	Power	Ground
C39	3P3V	3.3V_FMC	N/A	N/A	N/A	N/A	FMC 3.3 V power input (supplied from the carrier board)
C40	GND	GND	GND	GND	GND	Power	Ground
D1	PG_C2M	FMC_PG_C2M_3V3	N/A	N/A	N/A	N/A	FMC PG_C2M signal (carrier board power-good)
D2	GND	GND	GND	GND	GND	Power	Ground
D3	GND	GND	GND	GND	GND	Power	Ground
D4	GBTCLK0_M2C_P	GTSL_1A_REFCLK_RX_P	GTSL_1A_REFCLK_RX_P	REFCLK_GTSL_1A_RX_P	P25	Input	Transceiver Bank 1A Regional Reference Clock (P)
D5	GBTCLK0_M2C_N	GTSL_1A_REFCLK_RX_N	GTSL_1A_REFCLK_RX_N	REFCLK_GTSL_1A_RX_N	P24	Input	Transceiver Bank 1A Regional Reference Clock (N)
D6	GND	GND	GND	GND	GND	Power	Ground
D7	GND	GND	GND	GND	GND	Power	Ground
D8	LA01_P_CC	HSIO_2A_T_IO2_P	HSIO_2A_T_IO2_P	IOB,DIFF_IO_2A_T2P	N6	I/O	HSIO Bank 2A_T IO2 differential (P) / single-ended
D9	LA01_N_CC	HSIO_2A_T_IO2_N	HSIO_2A_T_IO2_N	IOB,DIFF_IO_2A_T2N	N7	I/O	HSIO Bank 2A_T IO2 differential (N) / single-ended
D10	GND	GND	GND	GND	GND	Power	Ground
D11	LA05_P	HSIO_2A_B_IO17_P	HSIO_2A_B_IO17_P	IOB,DIFF_IO_2A_B17P	Y2	I/O	HSIO Bank 2A_B IO17 differential (P) / single-ended
D12	LA05_N	HSIO_2A_B_IO17_N	HSIO_2A_B_IO17_N	IOB,DIFF_IO_2A_B17N	AA1	I/O	HSIO Bank 2A_B IO17 differential (N) / single-ended
D13	GND	GND	GND	GND	GND	Power	Ground
D14	LA09_P	HSIO_2A_T_IO23_P	HSIO_2A_T_IO23_P	IOB,DIFF_IO_2A_T23P	V1	I/O	HSIO Bank 2A_T IO23 differential (P) / single-ended

Pin No.	FMC Vita 57.1	Carrier Board Signal Name	SoM Pin Name	FPGA Pin Name	FPGA Pin	FPGA IO	Description
D15	LA09_N	HSIO_2A_T_IO23_N	HSIO_2A_T_IO23_N	IOB,DIFF_IO_2A_T23N	V2	I/O	HSIO Bank 2A_T IO23 differential (N) / single-ended
D16	GND	GND	GND	GND	GND	Power	Ground
D17	LA13_P	HSIO_2A_T_IO6_P	HSIO_2A_T_IO6_P	IOB,DIFF_IO_2A_T6P	V6	I/O	HSIO Bank 2A_T IO6 differential (P) / single-ended
D18	LA13_N	HSIO_2A_T_IO6_N	HSIO_2A_T_IO6_N	IOB,DIFF_IO_2A_T6N	W5	I/O	HSIO Bank 2A_T IO6 differential (N) / single-ended
D19	GND	GND	GND	GND	GND	Power	Ground
D20	LA17_P_CC	HSIO_2A_T_IO20_P	HSIO_2A_T_IO20_P	IOB,DIFF_IO_2A_T20P	R1	I/O	HSIO Bank 2A_T IO20 differential (P) / single-ended
D21	LA17_N_CC	HSIO_2A_T_IO20_N	HSIO_2A_T_IO20_N	IOB,DIFF_IO_2A_T20N	P2	I/O	HSIO Bank 2A_T IO20 differential (N) / single-ended
D22	GND	GND	GND	GND	GND	Power	Ground
D23	LA23_P	HSIO_2A_B_IO14_P	HSIO_2A_B_IO14_P	IOB,DIFF_IO_2A_B14P	AF1	I/O	HSIO Bank 2A_B IO14 differential (P) / single-ended
D24	LA23_N	HSIO_2A_B_IO14_N	HSIO_2A_B_IO14_N	IOB,DIFF_IO_2A_B14N	AE2	I/O	HSIO Bank 2A_B IO14 differential (N) / single-ended
D25	GND	GND	GND	GND	GND	Power	Ground
D26	LA26_P	HSIO_2A_T_IO8_P	HSIO_2A_T_IO8_P	IOB,DIFF_IO_2A_T8P	P5	I/O	HSIO Bank 2A_T IO8 differential (P) / single-ended
D27	LA26_N	HSIO_2A_T_IO8_N	HSIO_2A_T_IO8_N	IOB,DIFF_IO_2A_T8N	P4	I/O	HSIO Bank 2A_T IO8 differential (N) / single-ended
D28	GND	GND	GND	GND	GND	Power	Ground
D29	TCK	N/A	N/A	N/A	N/A	N/A	Not connected
D30	TDI	N/A	N/A	N/A	N/A	N/A	Not connected
D31	TDO	N/A	N/A	N/A	N/A	N/A	Not connected
D32	3P3VAUX	3.3V_FMC	N/A	N/A	N/A	N/A	FMC 3P3VAUX power input (3.3 V supplied from carrier board)
D33	TMS	N/A	N/A	N/A	N/A	N/A	Not connected
D34	TRST_L	N/A	N/A	N/A	N/A	N/A	Not connected
D35	GA1	FMC_GA1	N/A	N/A	N/A	N/A	FMC GA1 signal (pulled down on the carrier board)
D36	3P3V	3.3V_FMC	N/A	N/A	N/A	N/A	FMC 3.3 V power input (supplied from the carrier board)
D37	GND	GND	GND	GND	GND	Power	Ground
D38	3P3V	3.3V_FMC	N/A	N/A	N/A	N/A	FMC 3.3 V power input (supplied from the carrier board)
D39	GND	GND	GND	GND	GND	Power	Ground
D40	3P3V	3.3V_FMC	N/A	N/A	N/A	N/A	FMC 3.3 V power input (supplied from the carrier board)
E1	GND	GND	GND	GND	GND	Power	Ground
E2	HA01_P_CC	N/A	N/A	N/A	N/A	N/A	Not connected
E3	HA01_N_CC	N/A	N/A	N/A	N/A	N/A	Not connected
E4	GND	GND	GND	GND	GND	Power	Ground
E5	GND	GND	GND	GND	GND	Power	Ground
E6	HA05_P	N/A	N/A	N/A	N/A	N/A	Not connected
E7	HA05_N	N/A	N/A	N/A	N/A	N/A	Not connected
E8	GND	GND	GND	GND	GND	Power	Ground
E9	HA09_P	N/A	N/A	N/A	N/A	N/A	Not connected
E10	HA09_N	N/A	N/A	N/A	N/A	N/A	Not connected
E11	GND	GND	GND	GND	GND	Power	Ground
E12	HA13_P	N/A	N/A	N/A	N/A	N/A	Not connected
E13	HA13_N	N/A	N/A	N/A	N/A	N/A	Not connected
E14	GND	GND	GND	GND	GND	Power	Ground
E15	HA16_P	N/A	N/A	N/A	N/A	N/A	Not connected
E16	HA16_N	N/A	N/A	N/A	N/A	N/A	Not connected
E17	GND	GND	GND	GND	GND	Power	Ground
E18	HA20_P	N/A	N/A	N/A	N/A	N/A	Not connected
E19	HA20_N	N/A	N/A	N/A	N/A	N/A	Not connected
E20	GND	GND	GND	GND	GND	Power	Ground
E21	HB03_P	N/A	N/A	N/A	N/A	N/A	Not connected
E22	HB03_N	N/A	N/A	N/A	N/A	N/A	Not connected
E23	GND	GND	GND	GND	GND	Power	Ground
E24	HB05_P	N/A	N/A	N/A	N/A	N/A	Not connected
E25	HB05_N	N/A	N/A	N/A	N/A	N/A	Not connected
E26	GND	GND	GND	GND	GND	Power	Ground
E27	HB09_P	N/A	N/A	N/A	N/A	N/A	Not connected

Pin No.	FMC Vita 57.1	Carrier Board Signal Name	SoM Pin Name	FPGA Pin Name	FPGA Pin	FPGA IO	Description
E28	HB09_N	N/A	N/A	N/A	N/A	N/A	Not connected
E29	GND	GND	GND	GND	GND	Power	Ground
E30	HB13_P	N/A	N/A	N/A	N/A	N/A	Not connected
E31	HB13_N	N/A	N/A	N/A	N/A	N/A	Not connected
E32	GND	GND	GND	GND	GND	Power	Ground
E33	HB19_P	N/A	N/A	N/A	N/A	N/A	Not connected
E34	HB19_N	N/A	N/A	N/A	N/A	N/A	Not connected
E35	GND	GND	GND	GND	GND	Power	Ground
E36	HB21_P	N/A	N/A	N/A	N/A	N/A	Not connected
E37	HB21_N	N/A	N/A	N/A	N/A	N/A	Not connected
E38	GND	GND	GND	GND	GND	Power	Ground
E39	VADJ	FMC_VADJ	N/A	N/A	N/A	N/A	FMC I/O voltage (1.2 V supplied from the carrier board)
E40	GND	GND	GND	GND	GND	Power	Ground
F1	PG_M2C	FMC_PG_M2C_3V3	HVIO_5A_IO11	HVIO_5A_IO11	AH18	Input, 3.3V	FMC PG_M2C signal
F2	GND	GND	GND	GND	GND	Power	Ground
F3	GND	GND	GND	GND	GND	Power	Ground
F4	HA00_P_CC	N/A	N/A	N/A	N/A	N/A	Not connected
F5	HA00_N_CC	N/A	N/A	N/A	N/A	N/A	Not connected
F6	GND	GND	GND	GND	GND	Power	Ground
F7	HA04_P	N/A	N/A	N/A	N/A	N/A	Not connected
F8	HA04_N	N/A	N/A	N/A	N/A	N/A	Not connected
F9	GND	GND	GND	GND	GND	Power	Ground
F10	HA08_P	N/A	N/A	N/A	N/A	N/A	Not connected
F11	HA08_N	N/A	N/A	N/A	N/A	N/A	Not connected
F12	GND	GND	GND	GND	GND	Power	Ground
F13	HA12_P	N/A	N/A	N/A	N/A	N/A	Not connected
F14	HA12_N	N/A	N/A	N/A	N/A	N/A	Not connected
F15	GND	GND	GND	GND	GND	Power	Ground
F16	HA15_P	N/A	N/A	N/A	N/A	N/A	Not connected
F17	HA15_N	N/A	N/A	N/A	N/A	N/A	Not connected
F18	GND	GND	GND	GND	GND	Power	Ground
F19	HA19_P	N/A	N/A	N/A	N/A	N/A	Not connected
F20	HA19_N	N/A	N/A	N/A	N/A	N/A	Not connected
F21	GND	GND	GND	GND	GND	Power	Ground
F22	HB02_P	N/A	N/A	N/A	N/A	N/A	Not connected
F23	HB02_N	N/A	N/A	N/A	N/A	N/A	Not connected
F24	GND	GND	GND	GND	GND	Power	Ground
F25	HB04_P	N/A	N/A	N/A	N/A	N/A	Not connected
F26	HB04_N	N/A	N/A	N/A	N/A	N/A	Not connected
F27	GND	GND	GND	GND	GND	Power	Ground
F28	HB08_P	N/A	N/A	N/A	N/A	N/A	Not connected
F29	HB08_N	N/A	N/A	N/A	N/A	N/A	Not connected
F30	GND	GND	GND	GND	GND	Power	Ground
F31	HB12_P	N/A	N/A	N/A	N/A	N/A	Not connected
F32	HB12_N	N/A	N/A	N/A	N/A	N/A	Not connected
F33	GND	GND	GND	GND	GND	Power	Ground
F34	HB16_P	N/A	N/A	N/A	N/A	N/A	Not connected
F35	HB16_N	N/A	N/A	N/A	N/A	N/A	Not connected
F36	GND	GND	GND	GND	GND	Power	Ground
F37	HB20_P	N/A	N/A	N/A	N/A	N/A	Not connected
F38	HB20_N	N/A	N/A	N/A	N/A	N/A	Not connected
F39	GND	GND	GND	GND	GND	Power	Ground
F40	VADJ	FMC_VADJ	N/A	N/A	N/A	N/A	FMC I/O voltage (1.2 V supplied from the carrier board)
G1	GND	GND	GND	GND	GND	Power	Ground
G2	CLK1_M2C_P	HSIO_2A_T_IO19_CLK0_P	HSIO_2A_T_IO19_CLK0_P	IOB,DIFF_IO_2A_T19P	N2	I/O, Input	HSIO Bank 2A_T IO19 differential (P) / single-ended / CLK0 differential clock (P) / single-ended clock
G3	CLK1_M2C_N	HSIO_2A_T_IO19_CLK0_N	HSIO_2A_T_IO19_CLK0_N	IOB,DIFF_IO_2A_T19N	N1	I/O, Input	HSIO Bank 2A_T IO19 differential (N) / single-ended / CLK0 differential clock (N) / single-ended clock
G4	GND	GND	GND	GND	GND	Power	Ground
G5	GND	GND	GND	GND	GND	Power	Ground
G6	LA00_P_CC	HSIO_2A_T_IO1_P	HSIO_2A_T_IO1_P	IOB,DIFF_IO_2A_T1P	R7	I/O	HSIO Bank 2A_T IO1 differential (P) / single-ended

Pin No.	FMC Vita 57.1	Carrier Board Signal Name	SoM Pin Name	FPGA Pin Name	FPGA Pin	FPGA IO	Description
G7	LA00_N_CC	HSIO_2A_T_IO11_N	HSIO_2A_T_IO1_N	IOB,DIFF_IO_2A_T1N	P7	I/O	HSIO Bank 2A_T IO1 differential (N) / single-ended
G8	GND	GND	GND	GND	GND	Power	Ground
G9	LA03_P	HSIO_2A_B_IO22_P	HSIO_2A_B_IO22_P	IOB,DIFF_IO_2A_B22P	AK4	I/O	HSIO Bank 2A_B IO22 differential (P) / single-ended
G10	LA03_N	HSIO_2A_B_IO22_N	HSIO_2A_B_IO22_N	IOB,DIFF_IO_2A_B22N	AJ4	I/O	HSIO Bank 2A_B IO22 differential (N) / single-ended
G11	GND	GND	GND	GND	GND	Power	Ground
G12	LA08_P	HSIO_2A_B_IO13_P	HSIO_2A_B_IO13_P	IOB,DIFF_IO_2A_B13P	AG1	I/O	HSIO Bank 2A_B IO13 differential (P) / single-ended
G13	LA08_N	HSIO_2A_B_IO13_N	HSIO_2A_B_IO13_N	IOB,DIFF_IO_2A_B13N	AF2	I/O	HSIO Bank 2A_B IO13 differential (N) / single-ended
G14	GND	GND	GND	GND	GND	Power	Ground
G15	LA12_P	HSIO_2A_B_IO15_P	HSIO_2A_B_IO15_P	IOB,DIFF_IO_2A_B15P	AD2	I/O	HSIO Bank 2A_B IO15 differential (P) / single-ended
G16	LA12_N	HSIO_2A_B_IO15_N	HSIO_2A_B_IO15_N	IOB,DIFF_IO_2A_B15N	AE1	I/O	HSIO Bank 2A_B IO15 differential (N) / single-ended
G17	GND	GND	GND	GND	GND	Power	Ground
G18	LA16_P	HSIO_2A_T_IO14_P	HSIO_2A_T_IO14_P	IOB,DIFF_IO_2A_T14P	Y7	I/O	HSIO Bank 2A_T IO14 differential (P) / single-ended
G19	LA16_N	HSIO_2A_T_IO14_N	HSIO_2A_T_IO14_N	IOB,DIFF_IO_2A_T14N	Y6	I/O	HSIO Bank 2A_T IO14 differential (N) / single-ended
G20	GND	GND	GND	GND	GND	Power	Ground
G21	LA20_P	HSIO_2A_T_IO7_P	HSIO_2A_T_IO7_P	IOB,DIFF_IO_2A_T7P	N3	I/O	HSIO Bank 2A_T IO7 differential (P) / single-ended
G22	LA20_N	HSIO_2A_T_IO7_N	HSIO_2A_T_IO7_N	IOB,DIFF_IO_2A_T7N	P3	I/O	HSIO Bank 2A_T IO7 differential (N) / single-ended
G23	GND	GND	GND	GND	GND	Power	Ground
G24	LA22_P	HSIO_2A_T_IO12_P	HSIO_2A_T_IO12_P	IOB,DIFF_IO_2A_T12P	V3	I/O	HSIO Bank 2A_T IO12 differential (P) / single-ended
G25	LA22_N	HSIO_2A_T_IO12_N	HSIO_2A_T_IO12_N	IOB,DIFF_IO_2A_T12N	W3	I/O	HSIO Bank 2A_T IO12 differential (N) / single-ended
G26	GND	GND	GND	GND	GND	Power	Ground
G27	LA25_P	HSIO_2A_T_IO10_P	HSIO_2A_T_IO10_P	IOB,DIFF_IO_2A_T10P	U5	I/O	HSIO Bank 2A_T IO10 differential (P) / single-ended
G28	LA25_N	HSIO_2A_T_IO10_N	HSIO_2A_T_IO10_N	IOB,DIFF_IO_2A_T10N	T4	I/O	HSIO Bank 2A_T IO10 differential (N) / single-ended
G29	GND	GND	GND	GND	GND	Power	Ground
G30	LA29_P	HSIO_2A_T_IO16_P	HSIO_2A_T_IO16_P	IOB,DIFF_IO_2A_T16P	AB5	I/O	HSIO Bank 2A_T IO16 differential (P) / single-ended
G31	LA29_N	HSIO_2A_T_IO16_N	HSIO_2A_T_IO16_N	IOB,DIFF_IO_2A_T16N	AB6	I/O	HSIO Bank 2A_T IO16 differential (N) / single-ended
G32	GND	GND	GND	GND	GND	Power	Ground
G33	LA31_P	HSIO_2A_B_IO20_P	HSIO_2A_B_IO20_P	IOB,DIFF_IO_2A_B20P	AK7	I/O	HSIO Bank 2A_B IO20 differential (P) / single-ended
G34	LA31_N	HSIO_2A_B_IO20_N	HSIO_2A_B_IO20_N	IOB,DIFF_IO_2A_B20N	AJ8	I/O	HSIO Bank 2A_B IO20 differential (N) / single-ended
G35	GND	GND	GND	GND	GND	Power	Ground
G36	LA33_P	HSIO_2A_B_IO23_P	HSIO_2A_B_IO23_P	IOB,DIFF_IO_2A_B23P	AH2	I/O	HSIO Bank 2A_B IO23 differential (P) / single-ended
G37	LA33_N	HSIO_2A_B_IO23_N	HSIO_2A_B_IO23_N	IOB,DIFF_IO_2A_B23N	AG3	I/O	HSIO Bank 2A_B IO23 differential (N) / single-ended
G38	GND	GND	GND	GND	GND	Power	Ground
G39	VADJ	FMC_VADJ	N/A	N/A	N/A	N/A	FMC I/O voltage (1.2 V supplied from the carrier board)
G40	GND	GND	GND	GND	GND	Power	Ground
H1	VREF_A_M2C	N/A	N/A	N/A	N/A	N/A	Not connected
H2	PRSNT_M2C_L	FMC_PRSNT_B_3V3	HVIO_5A_IO12	HVIO_5A_IO12	AG21	Input, 3.3V	FMC PRSNT_M2C_L signal
H3	GND	GND	GND	GND	GND	Power	Ground
H4	CLK0_M2C_P	HSIO_2A_T_IO18_CLK1_P	HSIO_2A_T_IO18_CLK1_P	IOB,DIFF_IO_2A_T18P	AC6	I/O, Input	HSIO Bank 2A_T IO18 differential (P) / single-ended / CLK1 differential clock (P) / single-ended clock
H5	CLK0_M2C_N	HSIO_2A_T_IO18_CLK1_N	HSIO_2A_T_IO18_CLK1_N	IOB,DIFF_IO_2A_T18N	AC5	I/O, Input	HSIO Bank 2A_T IO18 differential (N) / single-ended / CLK1 differential clock (N) / single-ended clock
H6	GND	GND	GND	GND	GND	Power	Ground
H7	LA02_P	HSIO_2A_T_IO3_P	HSIO_2A_T_IO3_P	IOB,DIFF_IO_2A_T3P	T6	I/O	HSIO Bank 2A_T IO3 differential (P) / single-ended

Pin No.	FMC Vita 57.1	Carrier Board Signal Name	SoM Pin Name	FPGA Pin Name	FPGA Pin	FPGA IO	Description
H8	LA02_N	HSIO_2A_T_IO3_N	HSIO_2A_T_IO3_N	IOB,DIFF_IO_2A_T3N	T7	I/O	HSIO Bank 2A_T IO3 differential (N) / single-ended
H9	GND	GND	GND	GND	GND	Power	Ground
H10	LA04_P	HSIO_2A_B_IO21_P	HSIO_2A_B_IO21_P	IOB,DIFF_IO_2A_B21P	AJ5	I/O	HSIO Bank 2A_B IO21 differential (P) / single-ended
H11	LA04_N	HSIO_2A_B_IO21_N	HSIO_2A_B_IO21_N	IOB,DIFF_IO_2A_B21N	AK5	I/O	HSIO Bank 2A_B IO21 differential (N) / single-ended
H12	GND	GND	GND	GND	GND	Power	Ground
H13	LA07_P	HSIO_2A_B_IO19_P	HSIO_2A_B_IO19_P	IOB,DIFF_IO_2A_B19P	AK6	I/O	HSIO Bank 2A_B IO19 differential (P) / single-ended
H14	LA07_N	HSIO_2A_B_IO19_N	HSIO_2A_B_IO19_N	IOB,DIFF_IO_2A_B19N	AJ7	I/O	HSIO Bank 2A_B IO19 differential (N) / single-ended
H15	GND	GND	GND	GND	GND	Power	Ground
H16	LA11_P	HSIO_2A_B_IO16_P	HSIO_2A_B_IO16_P	IOB,DIFF_IO_2A_B16P	AC1	I/O	HSIO Bank 2A_B IO16 differential (P) / single-ended
H17	LA11_N	HSIO_2A_B_IO16_N	HSIO_2A_B_IO16_N	IOB,DIFF_IO_2A_B16N	AC2	I/O	HSIO Bank 2A_B IO16 differential (N) / single-ended
H18	GND	GND	GND	GND	GND	Power	Ground
H19	LA15_P	HSIO_2A_T_IO9_P	HSIO_2A_T_IO9_P	IOB,DIFF_IO_2A_T9P	T3	I/O	HSIO Bank 2A_T IO9 differential (P) / single-ended
H20	LA15_N	HSIO_2A_T_IO9_N	HSIO_2A_T_IO9_N	IOB,DIFF_IO_2A_T9N	R4	I/O	HSIO Bank 2A_T IO9 differential (N) / single-ended
H21	GND	GND	GND	GND	GND	Power	Ground
H22	LA19_P	HSIO_2A_T_IO24_P	HSIO_2A_T_IO24_P	IOB,DIFF_IO_2A_T24P	Y1	I/O	HSIO Bank 2A_T IO24 differential (P) / single-ended
H23	LA19_N	HSIO_2A_T_IO24_N	HSIO_2A_T_IO24_N	IOB,DIFF_IO_2A_T24N	W2	I/O	HSIO Bank 2A_T IO24 differential (N) / single-ended
H24	GND	GND	GND	GND	GND	Power	Ground
H25	LA21_P	HSIO_2A_T_IO13_P	HSIO_2A_T_IO13_P	IOB,DIFF_IO_2A_T13P	V7	I/O	HSIO Bank 2A_T IO13 differential (P) / single-ended
H26	LA21_N	HSIO_2A_T_IO13_N	HSIO_2A_T_IO13_N	IOB,DIFF_IO_2A_T13N	W7	I/O	HSIO Bank 2A_T IO13 differential (N) / single-ended
H27	GND	GND	GND	GND	GND	Power	Ground
H28	LA24_P	HSIO_2A_T_IO5_P	HSIO_2A_T_IO5_P	IOB,DIFF_IO_2A_T5P	V5	I/O	HSIO Bank 2A_T IO5 differential (P) / single-ended
H29	LA24_N	HSIO_2A_T_IO5_N	HSIO_2A_T_IO5_N	IOB,DIFF_IO_2A_T5N	U6	I/O	HSIO Bank 2A_T IO5 differential (N) / single-ended
H30	GND	GND	GND	GND	GND	Power	Ground
H31	LA28_P	HSIO_2A_T_IO15_P	HSIO_2A_T_IO15_P	IOB,DIFF_IO_2A_T15P	AA6	I/O	HSIO Bank 2A_T IO15 differential (P) / single-ended
H32	LA28_N	HSIO_2A_T_IO15_N	HSIO_2A_T_IO15_N	IOB,DIFF_IO_2A_T15N	AA7	I/O	HSIO Bank 2A_T IO15 differential (N) / single-ended
H33	GND	GND	GND	GND	GND	Power	Ground
H34	LA30_P	HSIO_2A_T_IO17_P	HSIO_2A_T_IO17_P	IOB,DIFF_IO_2A_T17P	AC7	I/O	HSIO Bank 2A_T IO17 differential (P) / single-ended
H35	LA30_N	HSIO_2A_T_IO17_N	HSIO_2A_T_IO17_N	IOB,DIFF_IO_2A_T17N	AD7	I/O	HSIO Bank 2A_T IO17 differential (N) / single-ended
H36	GND	GND	GND	GND	GND	Power	Ground
H37	LA32_P	HSIO_2A_B_IO24_P	HSIO_2A_B_IO24_P	IOB,DIFF_IO_2A_B24P	AJ3	I/O	HSIO Bank 2A_B IO24 differential (P) / single-ended
H38	LA32_N	HSIO_2A_B_IO24_N	HSIO_2A_B_IO24_N	IOB,DIFF_IO_2A_B24N	AH3	I/O	HSIO Bank 2A_B IO24 differential (N) / single-ended
H39	GND	GND	GND	GND	GND	Power	Ground
H40	VADJ	FMC_VADJ	N/A	N/A	N/A	N/A	FMC I/O voltage (1.2 V supplied from the carrier board)
J1	GND	GND	GND	GND	GND	Power	Ground
J2	CLK3_BIDIR_P	N/A	N/A	N/A	N/A	N/A	Not connected
J3	CLK3_BIDIR_N	N/A	N/A	N/A	N/A	N/A	Not connected
J4	GND	GND	GND	GND	GND	Power	Ground
J5	GND	GND	GND	GND	GND	Power	Ground
J6	HA03_P	N/A	N/A	N/A	N/A	N/A	Not connected
J7	HA03_N	N/A	N/A	N/A	N/A	N/A	Not connected
J8	GND	GND	GND	GND	GND	Power	Ground
J9	HA07_P	N/A	N/A	N/A	N/A	N/A	Not connected
J10	HA07_N	N/A	N/A	N/A	N/A	N/A	Not connected
J11	GND	GND	GND	GND	GND	Power	Ground
J12	HA11_P	N/A	N/A	N/A	N/A	N/A	Not connected

Pin No.	FMC Vita 57.1	Carrier Board Signal Name	SoM Pin Name	FPGA Pin Name	FPGA Pin	FPGA IO	Description
J13	HA11_N	N/A	N/A	N/A	N/A	N/A	Not connected
J14	GND	GND	GND	GND	GND	Power	Ground
J15	HA14_P	N/A	N/A	N/A	N/A	N/A	Not connected
J16	HA14_N	N/A	N/A	N/A	N/A	N/A	Not connected
J17	GND	GND	GND	GND	GND	Power	Ground
J18	HA18_P_CC	N/A	N/A	N/A	N/A	N/A	Not connected
J19	HA18_N_CC	N/A	N/A	N/A	N/A	N/A	Not connected
J20	GND	GND	GND	GND	GND	Power	Ground
J21	HA22_P	N/A	N/A	N/A	N/A	N/A	Not connected
J22	HA22_N	N/A	N/A	N/A	N/A	N/A	Not connected
J23	GND	GND	GND	GND	GND	Power	Ground
J24	HB01_P	N/A	N/A	N/A	N/A	N/A	Not connected
J25	HB01_N	N/A	N/A	N/A	N/A	N/A	Not connected
J26	GND	GND	GND	GND	GND	Power	Ground
J27	HB07_P	N/A	N/A	N/A	N/A	N/A	Not connected
J28	HB07_N	N/A	N/A	N/A	N/A	N/A	Not connected
J29	GND	GND	GND	GND	GND	Power	Ground
J30	HB11_P	N/A	N/A	N/A	N/A	N/A	Not connected
J31	HB11_N	N/A	N/A	N/A	N/A	N/A	Not connected
J32	GND	GND	GND	GND	GND	Power	Ground
J33	HB15_P	N/A	N/A	N/A	N/A	N/A	Not connected
J34	HB15_N	N/A	N/A	N/A	N/A	N/A	Not connected
J35	GND	GND	GND	GND	GND	Power	Ground
J36	HB18_P	N/A	N/A	N/A	N/A	N/A	Not connected
J37	HB18_N	N/A	N/A	N/A	N/A	N/A	Not connected
J38	GND	GND	GND	GND	GND	Power	Ground
J39	VIO_B_M2C	N/A	N/A	N/A	N/A	N/A	Not connected
J40	GND	GND	GND	GND	GND	Power	Ground
K1	VREF_B_M2C	N/A	N/A	N/A	N/A	N/A	Not connected
K2	GND	GND	GND	GND	GND	Power	Ground
K3	GND	GND	GND	GND	GND	Power	Ground
K4	CLK2_BIDIR_P	N/A	N/A	N/A	N/A	N/A	Not connected
K5	CLK2_BIDIR_N	N/A	N/A	N/A	N/A	N/A	Not connected
K6	GND	GND	GND	GND	GND	Power	Ground
K7	HA02_P	N/A	N/A	N/A	N/A	N/A	Not connected
K8	HA02_N	N/A	N/A	N/A	N/A	N/A	Not connected
K9	GND	GND	GND	GND	GND	Power	Ground
K10	HA06_P	N/A	N/A	N/A	N/A	N/A	Not connected
K11	HA06_N	N/A	N/A	N/A	N/A	N/A	Not connected
K12	GND	GND	GND	GND	GND	Power	Ground
K13	HA10_P	N/A	N/A	N/A	N/A	N/A	Not connected
K14	HA10_N	N/A	N/A	N/A	N/A	N/A	Not connected
K15	GND	GND	GND	GND	GND	Power	Ground
K16	HA17_P_CC	N/A	N/A	N/A	N/A	N/A	Not connected
K17	HA17_N_CC	N/A	N/A	N/A	N/A	N/A	Not connected
K18	GND	GND	GND	GND	GND	Power	Ground
K19	HA21_P	N/A	N/A	N/A	N/A	N/A	Not connected
K20	HA21_N	N/A	N/A	N/A	N/A	N/A	Not connected
K21	GND	GND	GND	GND	GND	Power	Ground
K22	HA23_P	N/A	N/A	N/A	N/A	N/A	Not connected
K23	HA23_N	N/A	N/A	N/A	N/A	N/A	Not connected
K24	GND	GND	GND	GND	GND	Power	Ground
K25	HB00_P_CC	N/A	N/A	N/A	N/A	N/A	Not connected
K26	HB00_N_CC	N/A	N/A	N/A	N/A	N/A	Not connected
K27	GND	GND	GND	GND	GND	Power	Ground
K28	HB06_P_CC	N/A	N/A	N/A	N/A	N/A	Not connected
K29	HB06_N_CC	N/A	N/A	N/A	N/A	N/A	Not connected

Pin No.	FMC Vita 57.1	Carrier Board Signal Name	SoM Pin Name	FPGA Pin Name	FPGA Pin	FPGA IO	Description
K30	GND	GND	GND	GND	GND	Power	Ground
K31	HB10_P	N/A	N/A	N/A	N/A	N/A	Not connected
K32	HB10_N	N/A	N/A	N/A	N/A	N/A	Not connected
K33	GND	GND	GND	GND	GND	Power	Ground
K34	HB14_P	N/A	N/A	N/A	N/A	N/A	Not connected
K35	HB14_N	N/A	N/A	N/A	N/A	N/A	Not connected
K36	GND	GND	GND	GND	GND	Power	Ground
K37	HB17_P_CC	N/A	N/A	N/A	N/A	N/A	Not connected
K38	HB17_N_CC	N/A	N/A	N/A	N/A	N/A	Not connected
K39	GND	GND	GND	GND	GND	Power	Ground
K40	VIO_B_M2C	N/A	N/A	N/A	N/A	N/A	Not connected

3. Hardware Setup

3.1. Inserting and Removing the microSD Card

To insert a microSD card, as shown Figure (a) below, align the card horizontally with the slot and push it in the direction of the arrow until it clicks into place.

To remove the microSD card, as shown in Figure (b), push the inserted card further in the direction of the arrow until it clicks. The card will partially eject, allowing you to grasp it with your fingers and gently pull it out.

(a) Inserting the microSD Card

(b) Removing the microSD Card

Figure 3-1 Inserting and Removing the microSD Card

The reference design to be written to the microSD card is available on our download site.

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3.2. **Power-On Procedure**

Power is supplied via USB Power Delivery (USB-PD). When 15 V is supplied from USB-PD, LED7 turns on. In this state, power is not supplied to the ICs on the board, including the SoM. When the power switch (SW9) is slid to the ON position, power is supplied to the board. While the board is powered, LED8 remains on.

Before connecting any FMC or HAT boards, an Altera FPGA Download Cable II, or MIPI flex cables to this product, disconnect the USB-PD cable and ensure that the board is not powered.

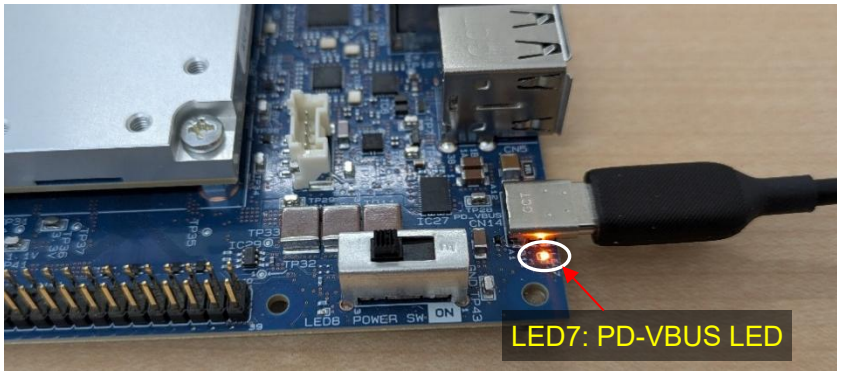


Figure 3-2 15 V (USB-PD) Applied / Power OFF State

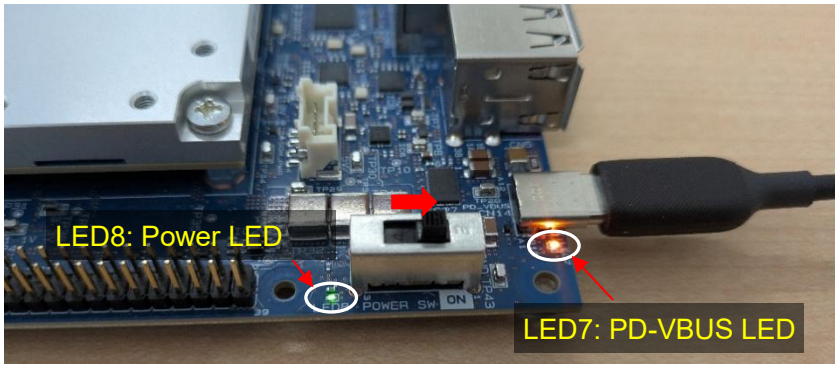


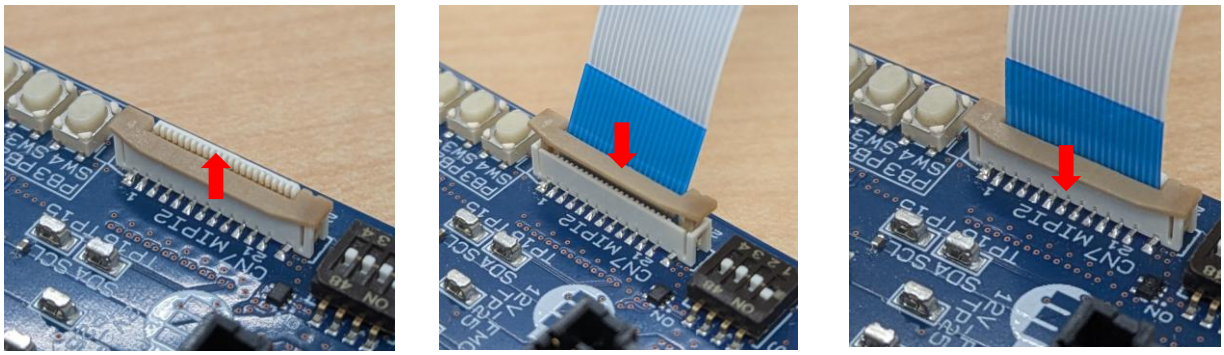
Figure 3-3 Power ON State

The power sequence is initiated by the power switch. **Do not power the board by plugging or unplugging the USB-PD cable while the power switch remains in the ON position.**
After use, disconnect the USB-PD cable and confirm that LED7 is off.

3.3. **Inserting and Removing the MIPI Cable**

To insert the MIPI cable into the connector, follow the steps shown below: (a) release the locking mechanism, (b) insert the MIPI cable, and (c) engage the locking mechanism to lock the cable in place.

To remove the cable, follow the reverse procedure.



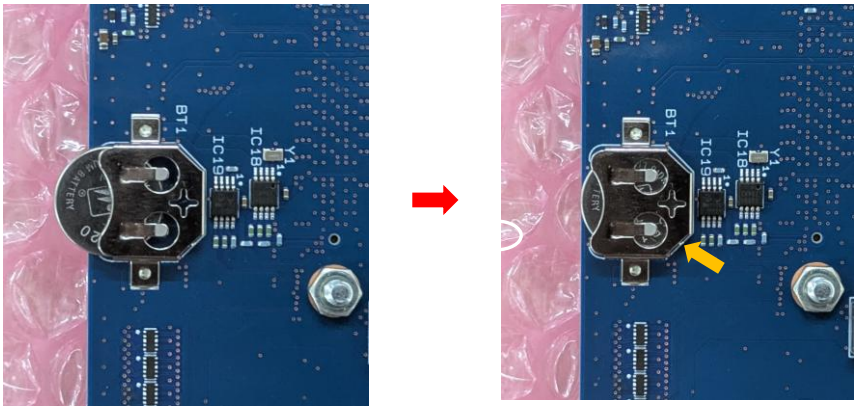
(a) Release the latch (b) Insert the MIPI cable (c) Lock the latch

Figure 3-4 Inserting and Removing the MIPI Cable

3.4. **Inserting and Removing the RTC Backup Battery**

Insert the RTC backup battery (CR1220) into the battery holder (BT1) on the back side of the development kit, as shown below, and press it in until it is flush with the board surface.
To remove the battery, insert a thin rod into the area indicated by the yellow arrow on the battery holder, and then pull out the battery.

Recommended battery model: CR1220 (Panasonic)
https://energy.panasonic.com/jp/business/products/lithium/coin-cr-standard/models/CR1220



(a) Insert the battery int the holder (b) Battery press-in position

Figure 3-5 Inserting and Removing the RTC Backup Battery

4. Board Dimensions

The external dimensions of this product are shown below. (Unit: mm)

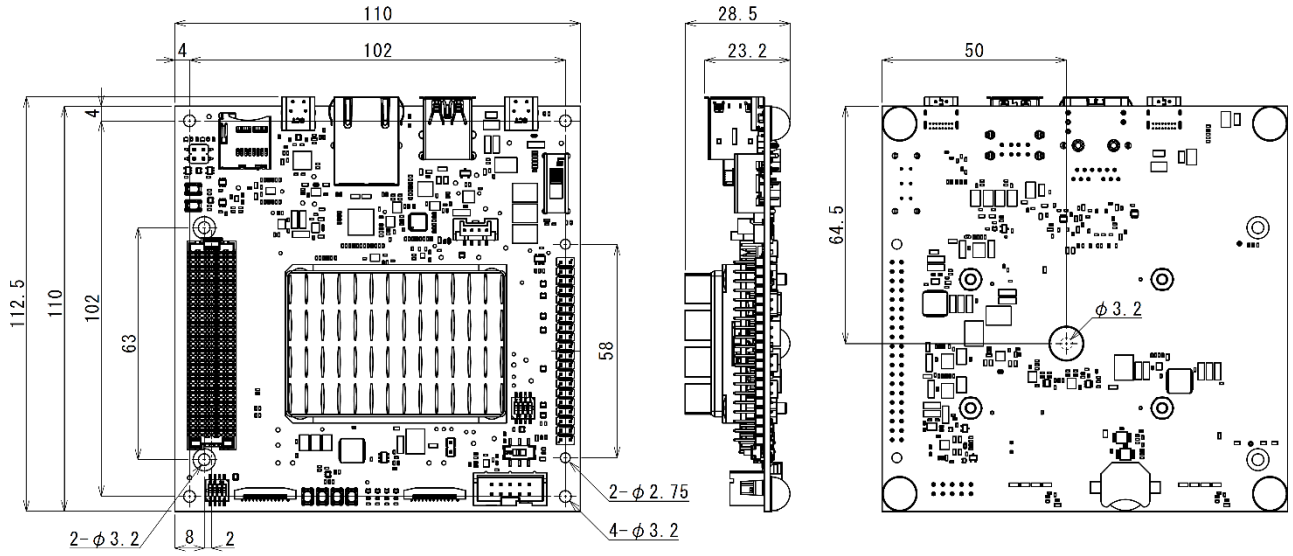


Figure 3-6 Outline Dimensions

5. **Revision History**

Ver.	Date	Description
1.0	2026/05/11	Initial Release