KElm-A5ESoM Mini
Hardware Manual

Ver.1.0

Kondo Electronics Industry Co., Ltd.

Introduction

Thank you for purchasing a KEIm product.

Before using this product, please carefully read this manual and related documents, and use this product correctly while observing all precautions.

CAUTION

- The contents of this manual are subject to change without prior notice. Please contact Kondo Electronics Industry or refer to its website for the latest information before using the product.
- This product uses components intended for general electronic equipment. Do not use it in applications requiring extremely high reliability, such as aerospace, nuclear control systems, or life-support medical equipment.
- This product has been developed and manufactured for use in Japan. If this product, or any product incorporating it, is exported, the customer is responsible for complying with the Foreign Exchange and Foreign Trade Act and all other applicable export laws and regulations, and for completing all necessary procedures.
- Always turn off the power before connecting or disconnecting cables to connectors other than LAN and USB.
- Do not use this product in environments with high levels of water, humidity, dust, or oil smoke.
- Unauthorized use or reproduction, in whole or in part, of this product's related documents is prohibited.
- All company and product names mentioned in these manual and related documents are trademarks or registered trademarks of their respective companies.

Contact Information

- For inquiries about this product, please contact us at the email address below:

keim-support@kd-group.co.jp

Table of contents

1. Overview

This document is a hardware manual that describes the hardware specifications of the “ KEIm-A5ESoM Mini ”, a System-on-Module (hereinafter referred as “SoM”) equipped with Agilex™ 5 SoC FPGA E-Series.

1.1. Product Features

This product is a compact FPGA-based embedded platform with the Agilex™ 5 SoC FPGA E-Series. In addition to the SoC FPGA, the module integrates LPDDR4 SDRAM as memory, eMMC as a storage device, and QSPI flash as a configuration ROM. The main feature of this product are as follows.

(1) Equipped with FPGA
Leveraging FPGA capabilities such as ultra-low latency and parallel processing, this product is well suited for the development of edge devices essential for IoT applications.

(2) Compact module size
The small form factor reduces the required mounting area, contributing to the miniaturization of end products and enabling more flexible product designs.

(3) Optimized compact configuration
By including only the necessary components, the module achieves a simple, flexible, and efficient design. This simplified configuration contributes to improved reliability and stability.

(4) Heat spreader mounted on the module
A heat spreader in mounted on the module to efficiently dissipate heat generated by the SoC FPGA, ensuring stable operation and simplifying thermal design.

(5) Long-term supply
The module is composed of components that support long-term availability, making it suitable for industrial equipment and other applications with long product lifecycles.

This product adopts a SoM architecture and is intended to be used in combination with a user-developed carrier board for specific applications. By using this module for the core processer and its peripheral circuits --areas that typically require significant design effort-- customers can reduce overall development time by designing application-specific carrier boards.

1.2. **Precautions for Use**

When using this product, see the following precautions:

- This product is provided as a SoM (System on Module) and cannot operate independently. A compatible carrier board must be prepared separately for use.

- The interfaces of this product depend on the carrier board design. Carefully verify signal levels, power specifications, and connection methods by referring to this manual and the device specification.

- Four specific screw holes inside the heat spreader are provided for evaluation purposes only.
  As the heat spreader is designed with priority on thinness and light weight, sufficient mechanical strength of these holes is not guaranteed. Therefore, these holes are not intended for use in end products.
  In addition, as these screw holes are through holes, use screws with a protrusion length of 3 mm or less to prevent contact with the board.

- Signals connected to the TPM are assigned to the LPDDR4 bank I/O of the SoM. Due to the specifications of the SoC FPGA EMIF, this function cannot be used when the HPS F2H bridge is enabled. When using this function, set the HPS F2H bridge to disabled.

1.3. Basic Specifications

The basic specifications of this product are shown below.

Table 1-1 Basic Specifications

Item		Description
SoC FPGA	Device Family	Agilex™ 5 SoC FPGA E-Series (M16A package) ·A5E 008B / 013B / 028B Agilex™ 3 SoC FPGA C-series (M16A package) ·A3C 100 / 135
Memory		4 GB, 32-bit LPDDR4 MT53E1G32D2FW-046 (Micron)
Configuration ROM		1 Gb Quad SPI Flash 256MByte (2Gbit) MT25QU01GBBB (Micron)
Storage		32GB eMMC MTFC32GAZAQHD (Micron)
TPM Module		SLB9672XU20FW1612XTMA1 (Infineon)
Clock	OSC_CLK_1	25MHz fixed oscillator
	LPDDR4 reference clock	100MHz fixed oscillator
Board-to-Board Connector	Type	240-pin board-to-board connector x 2
	Part Number	ADF6-60-03.5-L-4-2-A (Samtec)
	HPS I/O	Ethernet (RGMII) x1, USB (ULPI) x1, UART x1, I2C x1, up to 48 GPIOs (depending on HPS configuration)
	HSIO	Up to 120 pins (24 pins support 1.1 V bank)
	HVIO	Up to 40
	Transceiver (17 Gbps)	Up to 8 lanes (8 lanes for 028B, 4 lanes for other models)
	Debug I/F	JTAG
Power Supply		4.75V to 13.2 V
Power Consumption		TBD
Operating Temperature		-40°C~ +85°C
Dimensions		60 × 43 mm

1.4. **Board Layout**

The board layout of this product and the main components mounted on it are shown below.

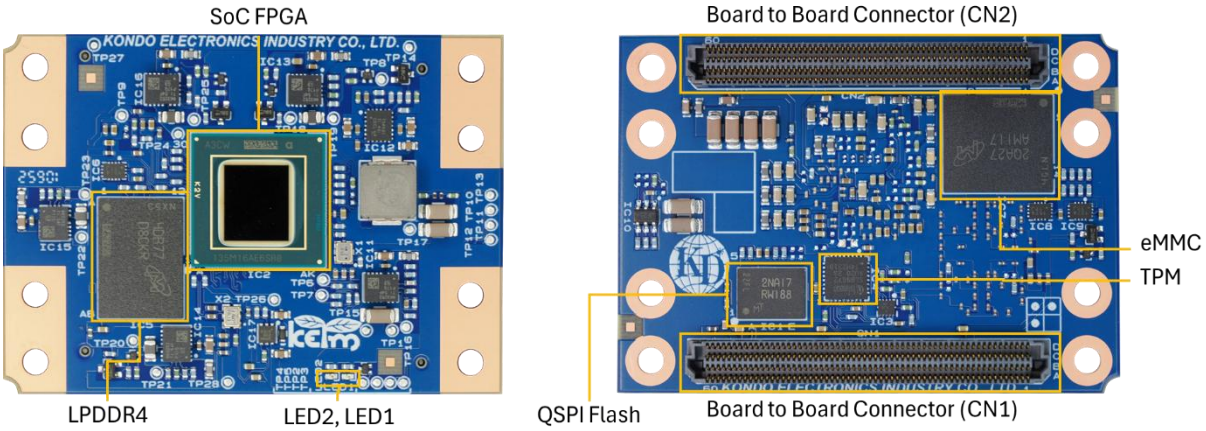


Figure 1-1 Board Layout

Table 1-2 List of Main Components

Reference	Name	Description
IC2	SoC FPGA	Agilex™ 5 SoC FPGA E-Series (M16A package) or Agilex™ 3 SoC FPGA C-series (M16A package)
IC1	QSPI Flash Memory	MT25QU01GBBB8E12-0SIT (Micron)
IC4	TPM Device	SLB9672XU20FW1612XTMA1 (Infineon)
IC5	LPDDR4 SDRAM	MT53E1G32D2FW-046IT:B (Micron)
IC15	eMMC	MTFC32GAZAQHD-IT (Micron) Can be used alternatively with a microSD card (mutually exclusive)
CN1, CN2	Board-to-Board Connector	ADF6-60-03.5-L-4-2-A (Samtec) 240-pin, 0.635 mm pitch, 4-row socket
LED1	CONF_DONE LED	Is lit when FPGA configuration is complete
LED2	Power LED	Is lit when power is supplied

1.5. **Board Block Diagram**

The block diagram of this product is shown below.

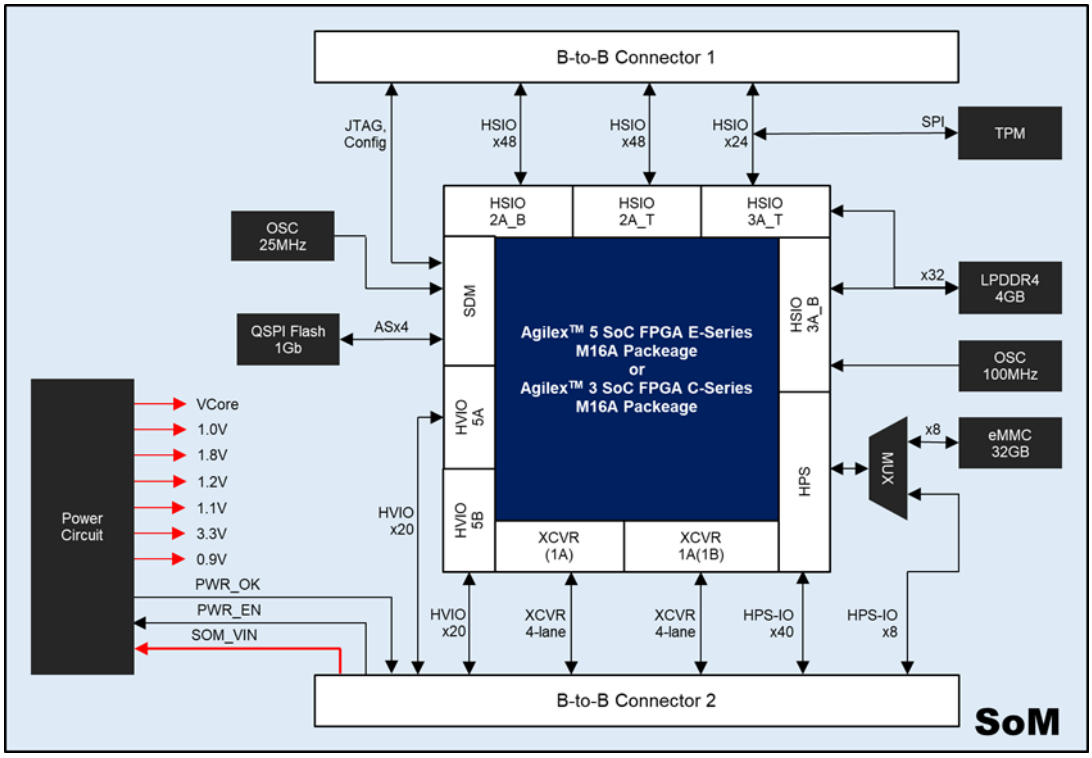


Figure 1-2 Board Block Diagram

2. Functional Specifications

2.1. Power Supply Circuit

This product is equipped with multiple DC/DC converters to supply the power required by the onboard devices.

In addition, a power sequencer controls the power-up and power-down sequences of each power rail. The configuration of the power supply circuit is shown below.

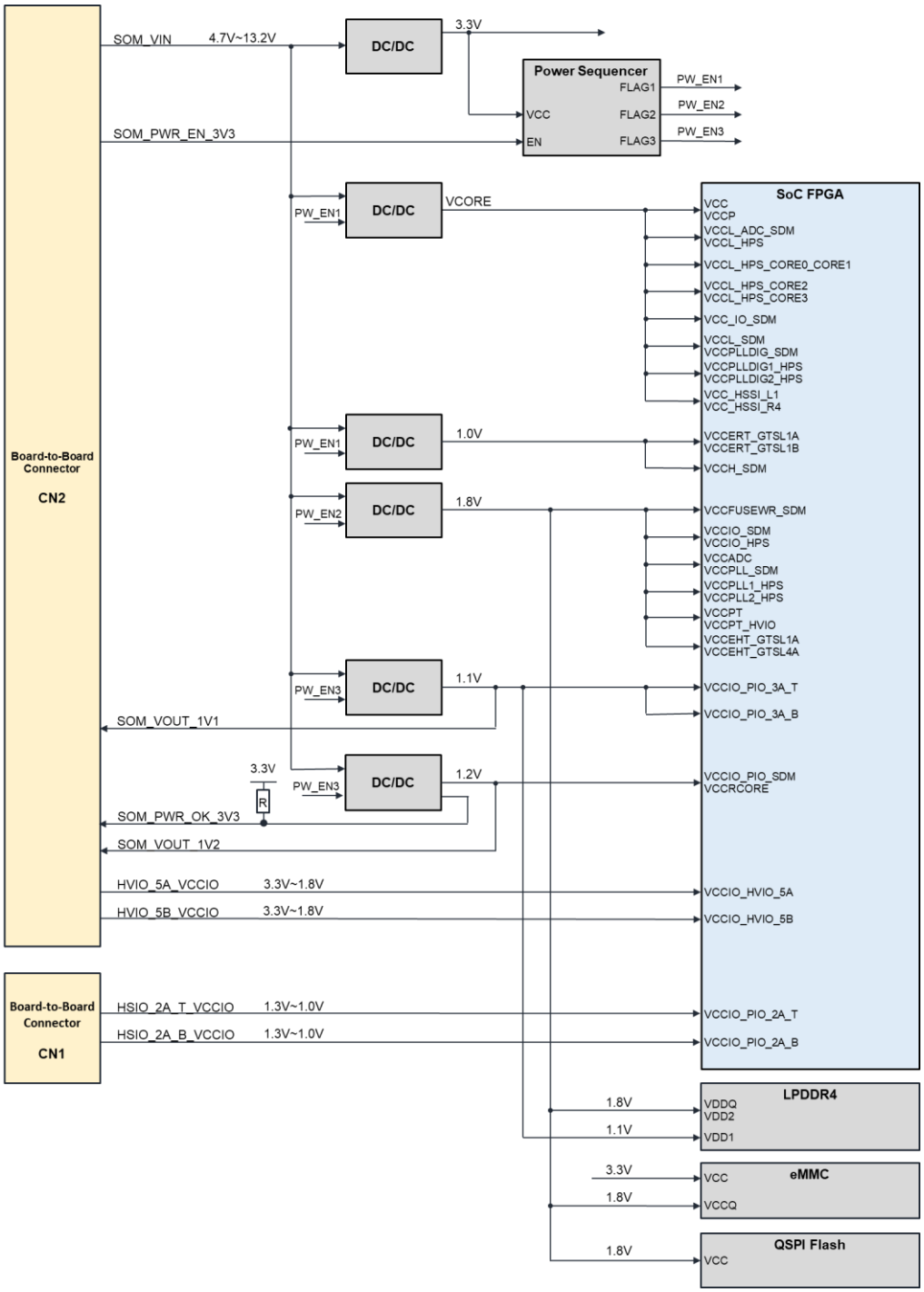


Figure 2-1 Power Supply Circuit

2.1.1. **Power-Up Sequence**

This product is equipped with a power sequence to satisfy the power sequencing requirements of the onboard devices. The power-up sequence is shown below.

Some VCCIO rails are supplied internally within the SoM. Power shall be supplied to external VCCIO rails and I/O pins only after the SOM_PWR_OK signal is High.

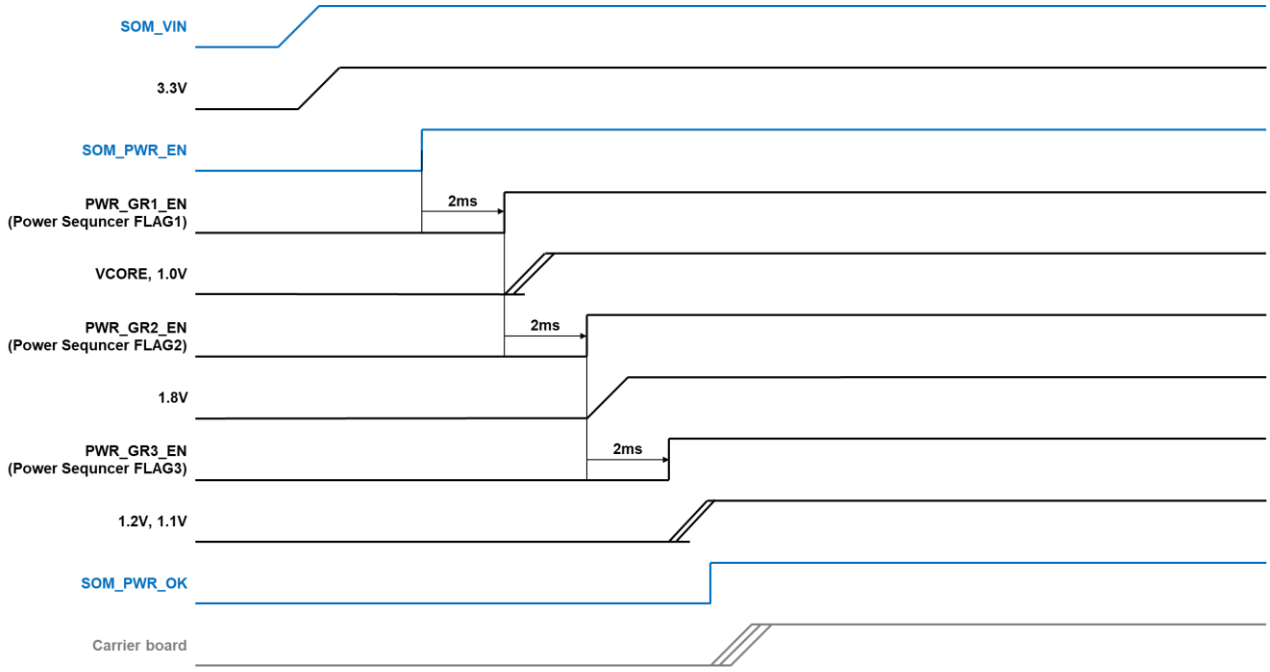


Figure 2-2 Power-Up Sequence

2.1.2. **Power-Down Sequence**

This product is equipped with a power sequencer to satisfy the power sequencing requirements of the onboard devices. The power-down sequence is shown below.

To ensure proper sequencing, keep SOM_VIN applied for approximately 10 ms after setting SOM_PWR_EN to Low.

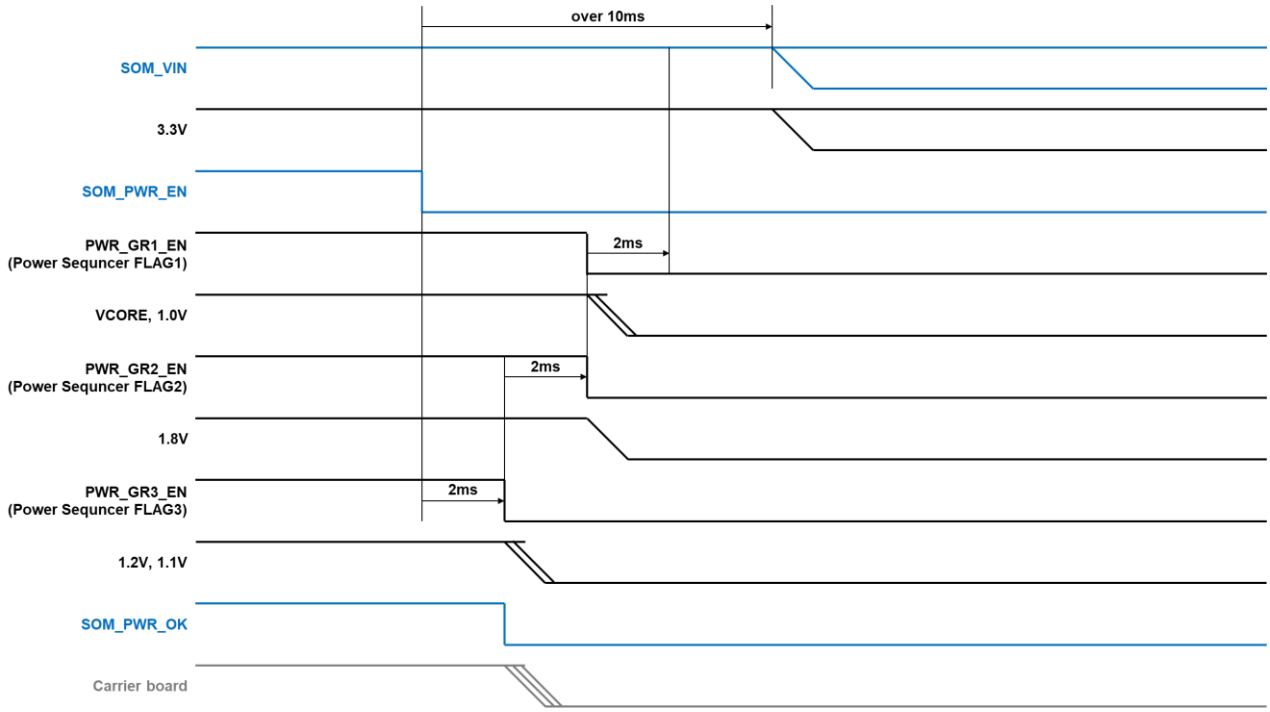


Figure 2-3 Power-Down Sequence

2.2. **Reset Circuit**

The configuration of the reset circuit and its pin assignments are below.
In this product, the eMMC reset signal is not connected to the SoC FPGA to maintain design flexibility. Since the eMMC must be reset at each cold reset, implement the necessary reset circuitry on the carrier board as required, and connect it to be SOM_EMMC_RST_B pin.

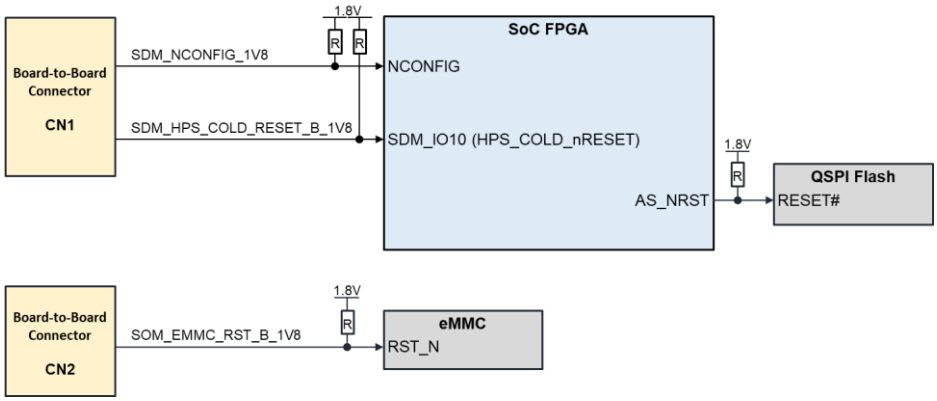


Figure 2-4 Reset Circuit

Table 2-1 Reset Circuit Pin Assignments

Signal Name	Direction	FPGA Pin No.	Voltage	Description
SDM_NCONFIG_1V8	Input	AG15	1.8V	NCONFIG input pin of the FPGA. Driving this pin Low and then High restarts FPGPA configuration.
SDM_HPS_COLD_RESET_B_1V8	Input	AH11	1.8V	Cold reset input pin of the HPS. Driving this pin Low initiates a cold reset.
SOM_EMMC_RST_B_1V8	Input	eMMC	1.8V	Reset input pin of the eMMC. Driving this pin Low resets the eMMC.

2.3. **Clock Circuit**

The configuration of the clock circuit and its pin assignments are shown below.
This product is equipped with a 100MHz reference clock for LPDDR4 and a 25MHz clock for the SDM.
Since a refence clock for the HPS is not provided on the module, it must be supplied externally.

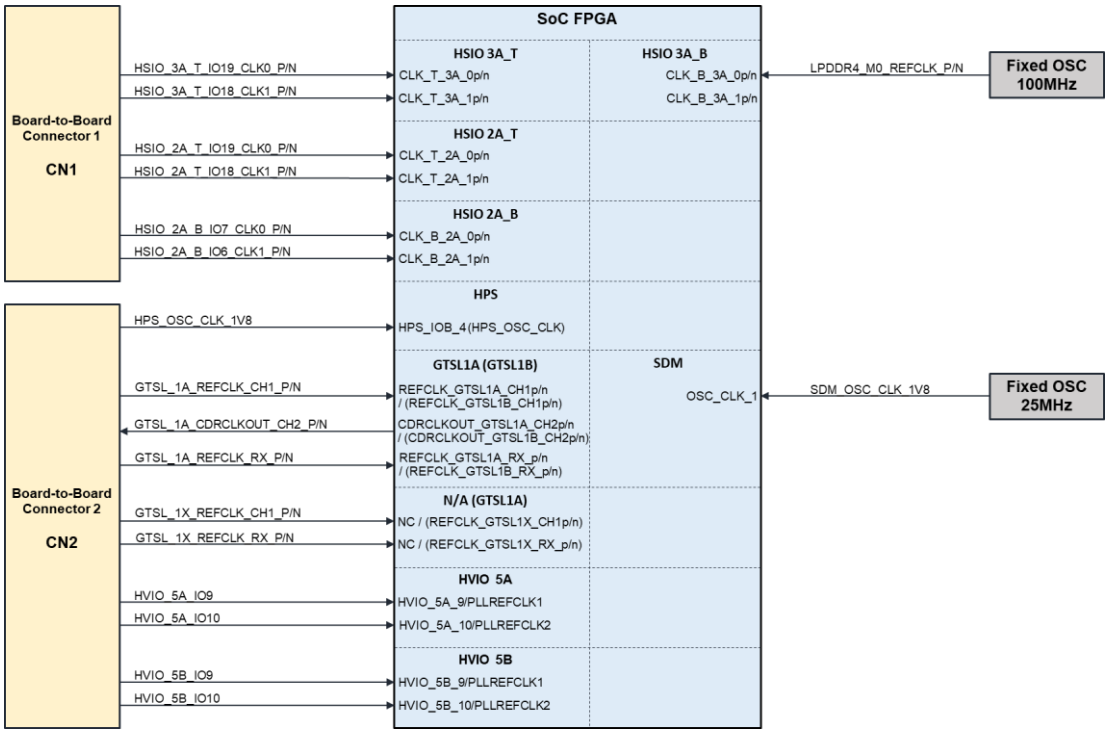


Figure 2-5 Clock Circuit

Table 2-2 Clock Circuit Pin Assignments

Signal Name	Direction	FPGA Pin No.	Voltage	Description
LPDDR4_M0_REFCLK_P	Input	A7	1.1V	LPDDR4 reference clock input (100MHz)
LPDDR4_M0_REFCLK_N	Input	B6	1.1V	LPDDR4 reference clock input (100MHz)
SDM_OSC_CLK_1V8	Input	AG11	1.8V	SDM PLL reference clock input (OSC_CLK_1, 25MHz)
HPS_IOA1_1V8	Input	B29	1.8V	HPS reference clock input or GPIO
HSIO_3A_T_IO19_CLK0_P	Input, I/O	D2	1.1V	FPGA clock input or FPGA I/O
HSIO_3A_T_IO19_CLK0_N	Input, I/O	E2	1.1V	FPGA clock input or FPGA I/O
HSIO_2A_T_IO19_CLK0_P	Input, I/O	N2	HSIO_2A_T_VCCIO	FPGA clock input or FPGA I/O
HSIO_2A_T_IO19_CLK0_N	Input, I/O	N1	HSIO_2A_T_VCCIO	FPGA clock input or FPGA I/O
HSIO_2A_T_IO18_CLK1_P	Input, I/O	AC6	HSIO_2A_T_VCCIO	FPGA clock input or FPGA I/O
HSIO_2A_T_IO18_CLK1_N	Input, I/O	AC5	HSIO_2A_T_VCCIO	FPGA clock input or FPGA I/O
HSIO_2A_B_IO7_CLK0_P	Input, I/O	AF3	HSIO_2A_B_VCCIO	FPGA clock input or FPGA I/O
HSIO_2A_B_IO7_CLK0_N	Input, I/O	AE4	HSIO_2A_B_VCCIO	FPGA clock input or FPGA I/O
HSIO_2A_B_IO6_CLK1_P	Input, I/O	AD5	HSIO_2A_B_VCCIO	FPGA clock input or FPGA I/O
HSIO_2A_B_IO6_CLK1_N	Input, I/O	AE5	HSIO_2A_B_VCCIO	FPGA clock input or FPGA I/O
GTSL_1A_CDRCLKOUT_CH2_N	Output	K25	-	Transceiver bank CDR recovered clock output
GTSL_1A_REFCLK_RX_P	Input	P25	-	Transceiver bank regional reference clock input
GTSL_1A_REFCLK_RX_N	Input	P24	-	Transceiver bank regional reference clock input

Signal Name	Direction	FPGA Pin No.	Voltage	Description
GTSL_1X_REFCLK_CH1_P	Input	V24	-	Transceiver bank local reference clock input*1
GTSL_1X_REFCLK_CH1_N	Input	V25	-	Transceiver bank local reference clock input*1
GTSL_1X_REFCLK_RX_P	Input	Y25	-	Transceiver bank regional reference clock input *1
GTSL_1X_REFCLK_RX_N	Input	Y24	-	Transceiver bank regional reference clock input *1
HVIO_5A_IO9	Input, I/O	AJ22	HVIO_5A_VCCIO	FPGA clock input or FPGA I/O
HVIO_5A_IO10	Input, I/O	AJ20	HVIO_5A_VCCIO	FPGA clock input or FPGA I/O
HVIO_5B_IO9	Input, I/O	AJ27	HVIO_5B_VCCIO	FPGA clock input or FPGA I/O
HVIO_5B_IO10	Input, I/O	AH27	HVIO_5B_VCCIO	FPGA clock input or FPGA I/O

*1 These pins are available only when the mounted device is the A5E 028B device. They are not connected for other devices.

2.4. Configuration Circuit

The configuration of the configuration circuit and its pin assignments are shown below.

The configuration mode can be selected by setting the MSEL2 and MSEL1 pins from the carrier board.

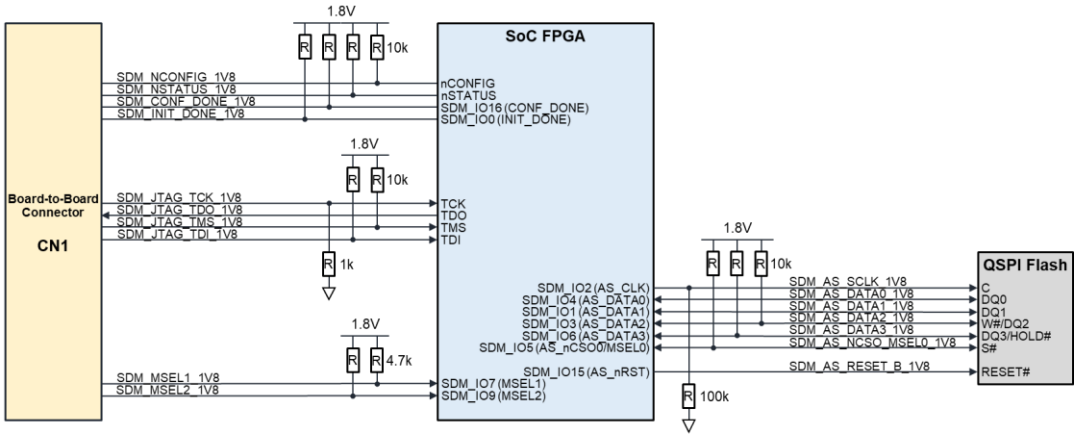


Figure 2-6 Configuration Circuit

Table 2-3 Configuration Circuit Pin Assignments

Signal Name	Direction	FPGA Pin No.	Voltage	Description
SDM_NCONFIG_1V8	Input	AG15	1.8V	FPGA reconfiguration input
SDM_NSTATUS_1V8	Input	AG16	1.8V	FPGA configuration status output
SDM_CONF_DONE_1V8	Output	AF9	1.8V	FPGA configuration completion output
SDM_INIT_DONE_1V8	Output	AG10	1.8V	FPGA initialization completion output
SDM_JTAG_TCK_1V8	Input	AF16	1.8V	JTAG test clock input
SDM_JTAG_TDO_1V8	Output	AE16	1.8V	JTAG test data output
SDM_JTAG_TMS_1V8	Input	AF17	1.8V	JTAG test mode input
SDM_JTAG_TDI_1V8	Input	AE17	1.8V	JTAG test data input
SDM_AS_RESET_B_1V8	Output	AG13	1.8V	QSPI flash reset output
SDM_AS_SCLK_1V8	Output	AH10	1.8V	QSPI flash clock input
SDM_AS_DATA0_1V8	I/O	AE10	1.8V	QSPI flash data 0
SDM_AS_DATA1_1V8	I/O	AK9	1.8V	QSPI flash data 1
SDM_AS_DATA2_1V8	I/O	AF14	1.8V	QSPI flash data 2
SDM_AS_DATA3_1V8	I/O	AG14	1.8V	QSPI flash data 3
SDM_AS_NCSO_MSEL0_1V8	Input, Output	AH12	1.8V	QSPI flash chip select output; functions as MSEL0 input during power-up
SDM_MSEL1_1V8	Input	AK10	1.8V	MSEL1 input
SDM_MSEL2_1V8	Input	AJ9	1.8V	MSEL2 input

2.4.1. **Configuration Modes**

The configuration mode can be selected by setting MSEL pins to High (logic 1) or Low (logic 0). The available settings are shown below.

Table 2-4 Configuration Modes

Mode Name	MSEL2	MSEL1	MSEL0	Description
JTAG Only Mode	1	1	1	Configuration is performed via JTAG only
AS Normal Mode	0	1	1	In Normal mode, configuration is performed from onboard QSPI flash.
AS Fast Mode	0	0	1	In Fast mode, configuration is performed from onboard QSPI flash.

2.5. HPS I/O

All 48 HPS I/O pins are connected to the board-to-board connectors, allowing flexible configuration depending on the system requirements. The pin assignments of the HPS I/O are shown below.

Table 2-5 HPS I/O Pin Assignments

SoM Signal Name	HPS Signa Name	FPGA Pin No.	Voltage	Description
HPS_IOA1_1V8	HPS_IOA_1	B29	1.8V	HPS IOA bit 1
HPS_ETH_INT_B_1V8	HPS_IOA_2	A27	1.8V	HPS IOA bit 2 / Ethernet Interrupt
HPS_UART_TXD_1V8	HPS_IOA_3	C27	1.8V	HPS IOA bit 3 / UART0 Transmit data
HPS_UART_RXD_1V8	HPS_IOA_4	F24	1.8V	HPS IOA bit 4 / UART0 Receive data
HPS_1PPS_OUT_1V8	HPS_IOA_5	B28	1.8V	HPS IOA bit 5 / EMAC2 1PPS trigger signal
HPS_1PPS_IN_1V8	HPS_IOA_6	F23	1.8V	HPS IOA bit 6 / EMAC2 1PPS signa
HPS_ETH_MDIO_1V8	HPS_IOA_7	D27	1.8V	HPS IOA bit 7 / EMAC2 serial data (MDIO)
HPS_ETH_MDC_1V8	HPS_IOA_8	E22	1.8V	HPS IOA bit 8 / EMAC2 serial clock(MDC)
HPS_I2C_SDA_1V8	HPS_IOA_9	C26	1.8V	HPS IOA bit 9 / I2C serial data
HPS_I2C_SCL_1V8	HPS_IOA_10	D22	1.8V	HPS IOA bit 10 / I2C serial clock
HPS_IOA11_1V8	HPS_IOA_11	A23	1.8V	HPS IOA bit 11
HPS_IOA12_1V8	HPS_IOA_12	A26	1.8V	HPS IOA bit 12
HPS_ULPI_CLK_1V8	HPS_IOA_13	D25	1.8V	HPS IOA bit 13 / USB1 Clock
HPS_ULPI_STP_1V8	HPS_IOA_14	B26	1.8V	HPS IOA bit 14 / USB1 Stop data
HPS_ULPI_DIR_1V8	HPS_IOA_15	B25	1.8V	HPS IOA bit 15 / USB1 Direction
HPS_ULPI_DATA0_1V8	HPS_IOA_16	E17	1.8V	HPS IOA bit 16 / USB1 Data bit0
HPS_ULPI_DATA1_1V8	HPS_IOA_17	A16	1.8V	HPS IOA bit 17 / USB1 Data bit1
HPS_ULPI_NXT_1V8	HPS_IOA_18	E16	1.8V	HPS IOA bit 18 / USB1 Next data
HPS_ULPI_DATA2_1V8	HPS_IOA_19	D24	1.8V	HPS IOA bit 19 / USB1 Data bit2
HPS_ULPI_DATA3_1V8	HPS_IOA_20	E21	1.8V	HPS IOA bit 20 / USB1 Data bit3
HPS_ULPI_DATA4_1V8	HPS_IOA_21	B23	1.8V	HPS IOA bit 21 / USB1 Data bit4
HPS_ULPI_DATA5_1V8	HPS_IOA_22	D20	1.8V	HPS IOA bit 22 / USB1 Data bit5
HPS_ULPI_DATA6_1V8	HPS_IOA_23	B24	1.8V	HPS IOA bit 23 / USB1 Data bit6
HPS_ULPI_DATA7_1V8	HPS_IOA_24	A24	1.8V	HPS IOA bit 24 / USB1 Data bit7
HPS_SDMMC_DATA0_1V8	HPS_IOB_1	D23	1.8V	HPS IOB bit 1 / SDMMC Data 0
HPS_SDMMC_DATA1_1V8	HPS_IOB_2	C25	1.8V	HPS IOB bit 2 / SDMMC Data 1
HPS_SDMMC_CLK_1V8	HPS_IOB_3	A18	1.8V	HPS IOB bit 3 / SDMMC Clock
HPS_OSC_CLK_1V8	HPS_IOB_4	C20	1.8V	HPS IOB bit 4 / Clock input
HPS_IOB5_1V8	HPS_IOB_5	A17	1.8V	HPS IOB bit 5
HPS_SDMMC_DATA2_1V8	HPS_IOB_6	C21	1.8V	HPS IOB bit 6 / SDMMC Data 2
HPS_SDMMC_DATA3_1V8	HPS_IOB_7	C23	1.8V	HPS IOB bit 7 / SDMMC Data 3
HPS_SDMMC_CMD_1V8	HPS_IOB_8	E20	1.8V	HPS IOB bit 8 / SDMMC Command
HPS_IOB9_1V8	HPS_IOB_9	C22	1.8V	HPS IOB bit 9
HPS_IOB10_1V8	HPS_IOB_10	D19	1.8V	HPS IOB bit 10
HPS_IOB11_1V8	HPS_IOB_11	B21	1.8V	HPS IOB bit 11
HPS_IOB12_1V8	HPS_IOB_12	A22	1.8V	HPS IOB bit 12
HPS_RGMII_TX_CLK_1V8	HPS_IOB_13	B16	1.8V	HPS IOB bit 13 / EMAC2 Transmit Clock
HPS_RGMII_TX_CTRL_1V8	HPS_IOB_14	B18	1.8V	HPS IOB bit 14 / EMAC2 Transmit Control
HPS_RGMII_RX_CLK_1V8	HPS_IOB_15	E19	1.8V	HPS IOB bit 15 / EMAC2 Receive Clock
HPS_RGMII_RX_CTRL_1V8	HPS_IOB_16	B20	1.8V	HPS IOB bit 16 / EMAC2 Receive Control
HPS_RGMII_TXD0_1V8	HPS_IOB_17	C18	1.8V	HPS IOB bit 17 / EMAC2 Transmit Data bit0
HPS_RGMII_TXD1_1V8	HPS_IOB_18	A21	1.8V	HPS IOB bit 18 / EMAC2 Transmit Data bit1
HPS_RGMII_RXD0_1V8	HPS_IOB_19	D17	1.8V	HPS IOB bit 19 / EMAC2 Receive Data bit0
HPS_RGMII_RXD1_1V8	HPS_IOB_20	A19	1.8V	HPS IOB bit 20 / EMAC2 Receive Data bit1
HPS_RGMII_TXD2_1V8	HPS_IOB_21	D18	1.8V	HPS IOB bit 21 / EMAC2 Transmit Data bit2
HPS_RGMII_TXD3_1V8	HPS_IOB_22	B19	1.8V	HPS IOB bit 22 / EMAC2 Transmit Data bit3
HPS_RGMII_RXD2_1V8	HPS_IOB_23	C17	1.8V	HPS IOB bit 23 / EMAC2 Receive Data bit2
HPS_RGMII_RXD3_1V8	HPS_IOB_24	C16	1.8V	HPS IOB bit 24 / EMAC2 Receive Data bit3

2.6. **LPDDR4**

This product is equipped with a 32-bit, 4GB LPDDR4 SDRAM as system memory. This memory is connected to the FPGA EMIF (External Memory Interface) and can be used as system memory for the OS when the HPS is implemented. It can be used as frame memory for image processing or other purposes when the HPS is not used.

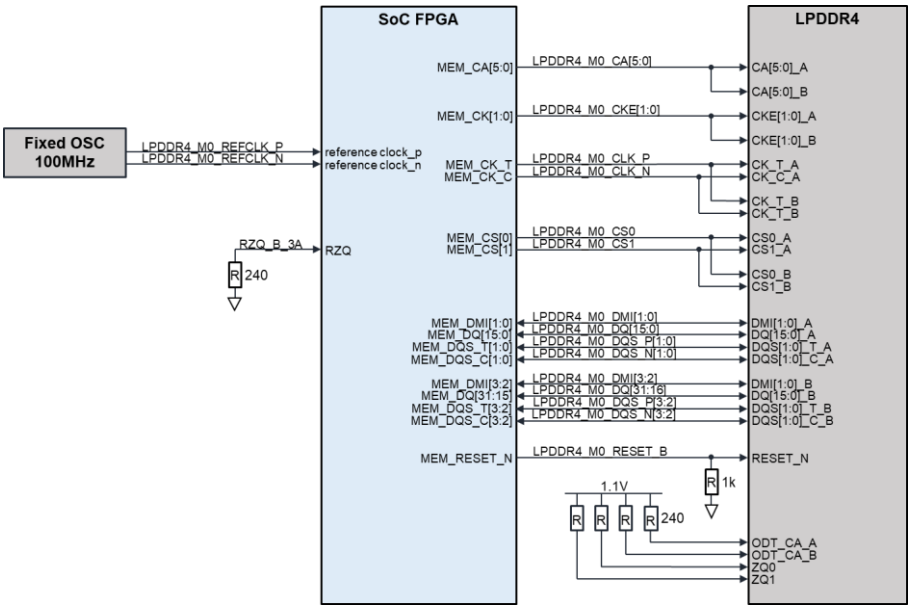


Figure 2-7 LPDDR4 Circuit

Table 2-6 LPDDR4 Cicuit Pin Assignments

Signal Name	Direction	FPGA Pin No.	Voltage	Description
LPDDR4_M0_CA0	Output	C2	1.1V	LPDDR4 command/address
LPDDR4_M0_CA1	Output	D3	1.1V	LPDDR4 command/address
LPDDR4_M0_CA2	Output	C3	1.1V	LPDDR4 command/address
LPDDR4_M0_CA3	Output	B3	1.1V	LPDDR4 command/address
LPDDR4_M0_CA4	Output	A6	1.1V	LPDDR4 command/address
LPDDR4_M0_CA5	Output	B5	1.1V	LPDDR4 command/address
LPDDR4_M0_CKE0	Output	A4	1.1V	LPDDR4 clock enable
LPDDR4_M0_CKE1	Output	B4	1.1V	LPDDR4 clock enable
LPDDR4_M0_CS0	Output	C7	1.1V	LPDDR4 chip select
LPDDR4_M0_CS1	Output	C6	1.1V	LPDDR4 chip select
LPDDR4_M0_REFCLK_P	Input	A7	1.1V	LPDDR4 reference clock
LPDDR4_M0_REFCLK_N	Input	B6	1.1V	LPDDR4 reference clock
RZQ_B_3A	I/O	E14	1.1V	Bank 3A RZQ pin
LPDDR4_M0_DMI0	I/O	B11	1.1V	LPDDR4 data mask inversion bit 0
LPDDR4_M0_DMI1	I/O	D13	1.1V	LPDDR4 data mask inversion bit 1
LPDDR4_M0_DMI2	I/O	K5	1.1V	LPDDR4 data mask inversion bit 2
LPDDR4_M0_DMI3	I/O	L7	1.1V	LPDDR4 data mask inversion bit 3
LPDDR4_M0_DQ0	I/O	B14	1.1V	LPDDR4 data bit 0
LPDDR4_M0_DQ1	I/O	A14	1.1V	LPDDR4 data bit 1
LPDDR4_M0_DQ2	I/O	A8	1.1V	LPDDR4 data bit 2
LPDDR4_M0_DQ3	I/O	B8	1.1V	LPDDR4 data bit 3
LPDDR4_M0_DQ4	I/O	B9	1.1V	LPDDR4 data bit 4
LPDDR4_M0_DQ5	I/O	A9	1.1V	LPDDR4 data bit 5
LPDDR4_M0_DQ6	I/O	A13	1.1V	LPDDR4 data bit 6

Signal Name	Direction	FPGA Pin No.	Voltage	Description
LPDDR4_M0_DQ7	I/O	B13	1.1V	LPDDR4 data bit 7
LPDDR4_M0_DQ8	I/O	C13	1.1V	LPDDR4 data bit 8
LPDDR4_M0_DQ9	I/O	D14	1.1V	LPDDR4 data bit 9
LPDDR4_M0_DQ10	I/O	D10	1.1V	LPDDR4 data bit 10
LPDDR4_M0_DQ11	I/O	C10	1.1V	LPDDR4 data bit 11
LPDDR4_M0_DQ12	I/O	D9	1.1V	LPDDR4 data bit 12
LPDDR4_M0_DQ13	I/O	C8	1.1V	LPDDR4 data bit 13
LPDDR4_M0_DQ14	I/O	D15	1.1V	LPDDR4 data bit 14
LPDDR4_M0_DQ15	I/O	C15	1.1V	LPDDR4 data bit 15
LPDDR4_M0_DQ16	I/O	M4	1.1V	LPDDR4 data bit 16
LPDDR4_M0_DQ17	I/O	M3	1.1V	LPDDR4 data bit 17
LPDDR4_M0_DQ18	I/O	J5	1.1V	LPDDR4 data bit 18
LPDDR4_M0_DQ19	I/O	H5	1.1V	LPDDR4 data bit 19
LPDDR4_M0_DQ20	I/O	G4	1.1V	LPDDR4 data bit 20
LPDDR4_M0_DQ21	I/O	H3	1.1V	LPDDR4 data bit 21
LPDDR4_M0_DQ22	I/O	L3	1.1V	LPDDR4 data bit 22
LPDDR4_M0_DQ23	I/O	L4	1.1V	LPDDR4 data bit 23
LPDDR4_M0_DQ24	I/O	M6	1.1V	LPDDR4 data bit 24
LPDDR4_M0_DQ25	I/O	L6	1.1V	LPDDR4 data bit 25
LPDDR4_M0_DQ26	I/O	H7	1.1V	LPDDR4 data bit 26
LPDDR4_M0_DQ27	I/O	H6	1.1V	LPDDR4 data bit 27
LPDDR4_M0_DQ28	I/O	G5	1.1V	LPDDR4 data bit 28
LPDDR4_M0_DQ29	I/O	G6	1.1V	LPDDR4 data bit 29
LPDDR4_M0_DQ30	I/O	M5	1.1V	LPDDR4 data bit 30
LPDDR4_M0_DQ31	I/O	N5	1.1V	LPDDR4 data bit 31
LPDDR4_M0_DQS_P0	I/O	B10	1.1V	LPDDR4 data strobe 0 (P)
LPDDR4_M0_DQS_N0	I/O	A11	1.1V	LPDDR4 data strobe 0 (N)
LPDDR4_M0_DQS_P1	I/O	D12	1.1V	LPDDR4 data strobe 1 (P)
LPDDR4_M0_DQS_N1	I/O	C11	1.1V	LPDDR4 data strobe 1 (N)
LPDDR4_M0_DQS_P2	I/O	J4	1.1V	LPDDR4 data strobe 2 (P)
LPDDR4_M0_DQS_N2	I/O	J3	1.1V	LPDDR4 data strobe 2 (N)
LPDDR4_M0_DQS_P3	I/O	K7	1.1V	LPDDR4 data strobe 3 (P)
LPDDR4_M0_DQS_N3	I/O	J7	1.1V	LPDDR4 data strobe 3 (N)
LPDDR4_M0_RESET_B	Output	E15	1.1V	LPDDR4 reset

2.7. **SDMMC**

This product is equipped with a 32 GB eMMC device as on-board storage. The eMMC is connected to the HPS SDMMC interface. By controlling the SOM_SDMMC_SEL_1V8 signal from the carrier board, the storage device can be switched between the onboard eMMC and an external storage device (such as a microSD card) on the carrier board.

The configuration of the SDMMC interface circuit and its pin assignments are shown below.

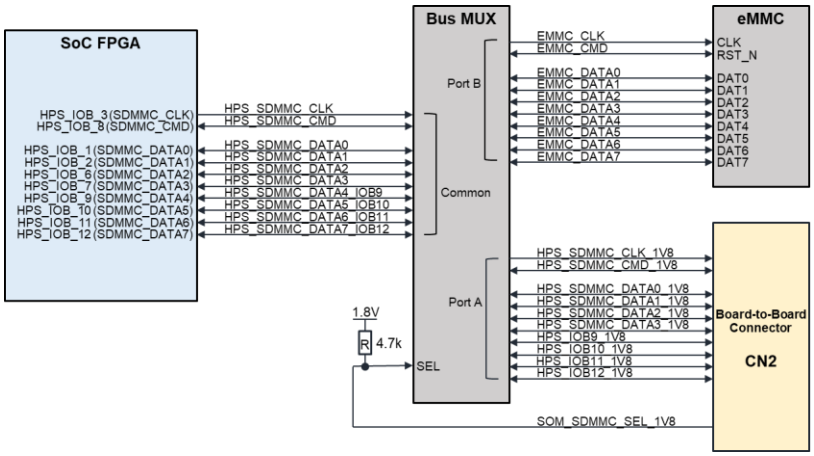


Figure 2-8 SDMMC Circuit

Table 2-7 SDMMC Circuit Pin Assignments

Signal Name	Direction	FPGA Pin No.	Voltage	Description
HPS_SDMMC_CLK	Output	A18	1.8V	SDMMC Clock
HPS_SDMMC_CMD	I/O	E20	1.8V	SDMMC Command
HPS_SDMMC_DATA0	I/O	D23	1.8V	SDMMC Data 0
HPS_SDMMC_DATA1	I/O	C25	1.8V	SDMMC Data 1
HPS_SDMMC_DATA2	I/O	C21	1.8V	SDMMC Data 2
HPS_SDMMC_DATA3	I/O	C23	1.8V	SDMMC Data 3
HPS_SDMMC_DATA4_IOB9	I/O	C22	1.8V	SDMMC Data 4. Can be used GPIO when using an SD card on the carrier board *1
HPS_SDMMC_DATA5_IOB10	I/O	D19	1.8V	SDMMC Data 5. Can be used GPIO when using an SD card on the carrier board *1
HPS_SDMMC_DATA6_IOB11	I/O	B21	1.8V	SDMMC Data 6. Can be used GPIO when using an SD card on the carrier board *1
HPS_SDMMC_DATA7_IOB12	I/O	A22	1.8V	SDMMC Data 7. Can be used GPIO when using an SD card on the carrier board *1
SOM_SDMMC_SEL_1V8	Input	Bus MUX	1.8V	SD/eMMC Selection signal. When set High, the onboard eMMC is selected; when set Low, the external storage device on the carrier board is selected.

*1 When an SD card is used on the carrier board, the SDMMC interface operates in 4-bit mode. Therefore,DATA4 to DATA7 can be used as GPIOs.

2.8. TPM

This product is equipped with a Trusted Platform Module (TPM) as a security feature. Using the TPM to securely generate and store cryptographic keys, unauthorized access to data can be prevented.

Usage Restrictions

The following restrictions apply when using this function:

- These signals connected to the TPM are assigned to the LPDDR4 bank I/Os of the SoM.
- Due to the EMIF specifications of the SoC FPGA, this function cannot be used when the HPS F2H bridge is enabled.

When using this function, disable the HPS F2H bridge.

The configuration of the TPM circuit and its pin assignments are shown below.

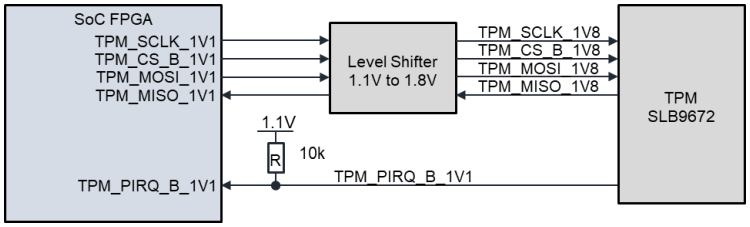


Figure 2-9 TPM Circuit

Figure 2-10 TPM Circuit Pin Assignments

Signal Name	Direction	FPGA Pin No.	Voltage	Description
TPM_SCLK_1V1	Output	J2	1.1V	TPM serial clock
TPM_CS_B_1V1	Output	K2	1.1V	TPM chip select
TPM_MOSI_1V1	Output	H1	1.1V	TPM serial data (MOSI)
TPM_MISO_1V1	Input	H2	1.1V	TPM serial data (MISO)
TPM_PIRQ_B_1V1	Input	E2	1.1V	TPM interrupt

2.9. On-Chip Voltage and Temperature Sensors

The signals of the on-chip voltage and temperature sensors integrated in the SoC FPGA are routed to the connectors so that these functions can be used.

The configuration of the on-chip voltage and temperature sensor circuits and their pin assignments are shown below.

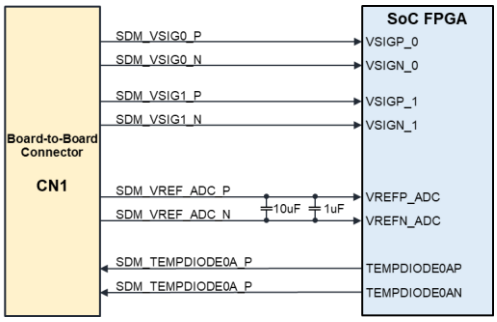


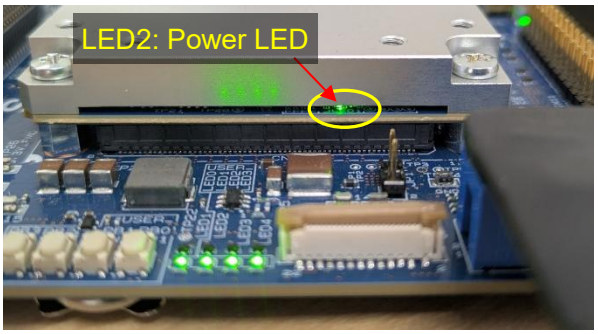
Figure 2-11 On-Chip Voltage and Temperature Sensor Circuits

Table 2-8 On-Chip Voltage and Temperature Sensor Circuit Pin Assignments

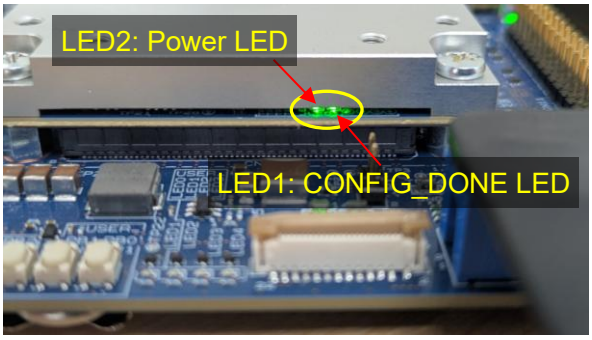
Signal Name	Direction	FPGA Pin No.	Voltage	Description
SDM_VSIG0_P	Input	AK14	Analog	On-chip voltage sensor channel 0 (P)
SDM_VSIG0_N	Input	AJ14	Analog	On-chip voltage sensor channel 0 (N)
SDM_VSIG1_P	Input	AK17	Analog	On-chip voltage sensor channel 1 (P)
SDM_VSIG1_N	Input	AK16	Analog	On-chip voltage sensor channel 2 (N)
SDM_VREF_ADC_P	Input	AJ15	Analog	On-chip ADC reference voltage (P)
SDM_VREF_ADC_N	Input	AK15	Analog	On-chip ADC reference voltage (N)
SDM_TEMPDIODE0A_P	Input	AH16	Analog	On-chip temperature sensor diode (P)
SDM_TEMPDIODE0A_N	Input	AH17	Analog	On-chip temperature sensor diode (N)

2.10. **Status LEDs**

This product is equipped with status LEDs for system monitoring. The functions of each LED are described below.



(a) Not configured



(b) Configuration complete

Table 2-9 Status LEDs

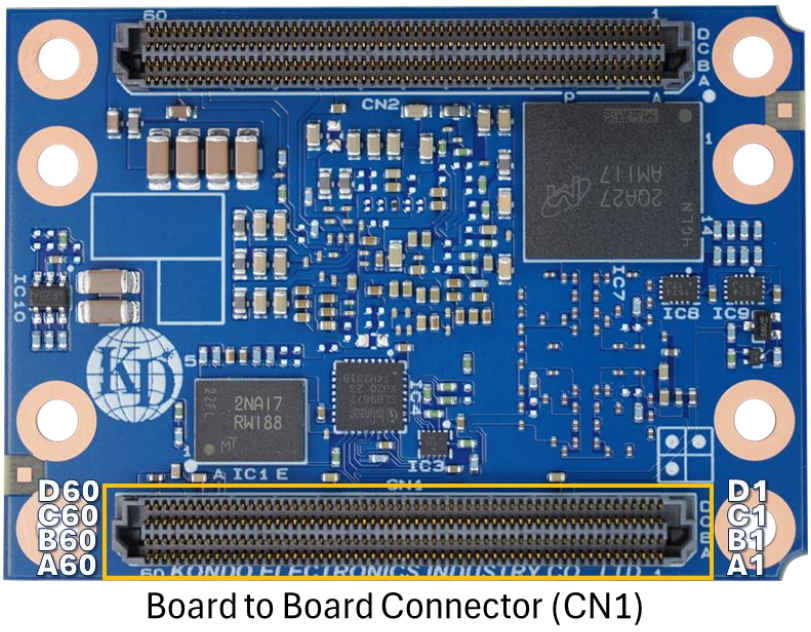
Reference	Name	Description
LED1	CONF_DONE LED	Indicates the configuration status. ON: Configuration completed OFF: Configuration not completed
LED2	Power LED	Indicates the power input status. This LED turns ON when power is supplied.

2.11. **Board-to-Board Connector 1 (CN1)**

The layout, pin assignment, and pin description of Board-to-Board Connector 1 are shown below.

Connector part number: ADF6-60-03.5-L-4-2-A-TR (Samtec)

Mating connector part number: ADM6-60-01.5-L-4-2-A-TR (Samtec)



Board to Board Connector (CN1)

Figure 2-12 Board-to-Board Connector 1 Layout

2.11.1. **CN1 Pin Assignment**

Table 2-10 CN1 Pin Assignment

Pin No.	A Row	B Row	C Row	D Row
1	HSIO_3A_T_IO22_N	GND	HSIO_3A_T_IO24_N	GND
2	HSIO_3A_T_IO22_P	HSIO_3A_T_IO23_N	HSIO_3A_T_IO24_P	HSIO_3A_T_IO19_CLK0_N
3	GND	HSIO_3A_T_IO23_P	GND	HSIO_3A_T_IO19_CLK0_P
4	HSIO_3A_T_IO18_CLK1_N	GND	HSIO_3A_T_IO16_N	GND
5	HSIO_3A_T_IO18_CLK1_P	HSIO_3A_T_IO21_N	HSIO_3A_T_IO16_P	HSIO_3A_T_IO14_N
6	GND	HSIO_3A_T_IO21_P	GND	HSIO_3A_T_IO14_P
7	HSIO_3A_T_IO17_N	GND	HSIO_3A_T_IO15_N	GND
8	HSIO_3A_T_IO17_P	HSIO_3A_T_IO20_N	HSIO_3A_T_IO15_P	HSIO_3A_T_IO13_N
9	GND	HSIO_3A_T_IO20_P	GND	HSIO_3A_T_IO13_P
10	RESERVED	GND	RESERVED	GND
11	RESERVED	RESERVED	RESERVED	SOM_VOUT_1V1
12	GND	RESERVED	GND	SOM_VOUT_1V1
13	HSIO_2A_T_IO1_N	GND	HSIO_2A_T_IO7_N	GND
14	HSIO_2A_T_IO1_P	HSIO_2A_T_IO2_N	HSIO_2A_T_IO7_P	HSIO_2A_T_IO19_CLK0_N
15	GND	HSIO_2A_T_IO2_P	GND	HSIO_2A_T_IO19_CLK0_P
16	HSIO_2A_T_IO4_N	GND	HSIO_2A_T_IO9_N	GND
17	HSIO_2A_T_IO4_P	HSIO_2A_T_IO8_N	HSIO_2A_T_IO9_P	HSIO_2A_T_IO20_N
18	GND	HSIO_2A_T_IO8_P	GND	HSIO_2A_T_IO20_P
19	HSIO_2A_T_IO3_N	GND	HSIO_2A_T_IO11_N	GND

Pin No.	A Row	B Row	C Row	D Row
20	HSIO_2A_T_IO3_P	HSIO_2A_T_IO10_N	HSIO_2A_T_IO11_P	HSIO_2A_T_IO21_N
21	GND	HSIO_2A_T_IO10_P	GND	HSIO_2A_T_IO21_P
22	HSIO_2A_T_IO5_N	GND	HSIO_2A_T_IO12_N	GND
23	HSIO_2A_T_IO5_P	HSIO_2A_T_IO16_N	HSIO_2A_T_IO12_P	HSIO_2A_T_IO22_N
24	GND	HSIO_2A_T_IO16_P	GND	HSIO_2A_T_IO22_P
25	HSIO_2A_T_IO15_N	GND	HSIO_2A_T_IO6_N	GND
26	HSIO_2A_T_IO15_P	HSIO_2A_T_IO13_N	HSIO_2A_T_IO6_P	HSIO_2A_T_IO23_N
27	GND	HSIO_2A_T_IO13_P	GND	HSIO_2A_T_IO23_P
28	HSIO_2A_T_IO17_N	GND	HSIO_2A_T_IO14_N	GND
29	HSIO_2A_T_IO17_P	HSIO_2A_T_IO18_CLK1_N	HSIO_2A_T_IO14_P	HSIO_2A_T_IO24_N
30	GND	HSIO_2A_T_IO18_CLK1_P	GND	HSIO_2A_T_IO24_P
31	HSIO_2A_T_VCCIO	GND	RESERVED	GND
32	HSIO_2A_T_VCCIO	SOM_VOUT_0V9	RESERVED	HSIO_2A_B_VCCIO
33	GND	SOM_VOUT_0V9	GND	HSIO_2A_B_VCCIO
34	HSIO_2A_B_IO4_N	GND	HSIO_2A_B_IO2_N	GND
35	HSIO_2A_B_IO4_P	HSIO_2A_B_IO1_N	HSIO_2A_B_IO2_P	HSIO_2A_B_IO17_N
36	GND	HSIO_2A_B_IO1_P	GND	HSIO_2A_B_IO17_P
37	HSIO_2A_B_IO6_CLK1_N	GND	HSIO_2A_B_IO3_N	GND
38	HSIO_2A_B_IO6_CLK1_P	HSIO_2A_B_IO5_N	HSIO_2A_B_IO3_P	HSIO_2A_B_IO18_N
39	GND	HSIO_2A_B_IO5_P	GND	HSIO_2A_B_IO18_P
40	HSIO_2A_B_IO23_N	GND	HSIO_2A_B_IO16_N	GND
41	HSIO_2A_B_IO23_P	HSIO_2A_B_IO7_CLK0_N	HSIO_2A_B_IO16_P	HSIO_2A_B_IO15_N
42	GND	HSIO_2A_B_IO7_CLK0_P	GND	HSIO_2A_B_IO15_P
43	HSIO_2A_B_IO8_N	GND	HSIO_2A_B_IO14_N	GND
44	HSIO_2A_B_IO8_P	HSIO_2A_B_IO24_N	HSIO_2A_B_IO14_P	HSIO_2A_B_IO13_N
45	GND	HSIO_2A_B_IO24_P	GND	HSIO_2A_B_IO13_P
46	HSIO_2A_B_IO11_N	GND	HSIO_2A_B_IO22_N	GND
47	HSIO_2A_B_IO11_P	HSIO_2A_B_IO10_N	HSIO_2A_B_IO22_P	HSIO_2A_B_IO21_N
48	GND	HSIO_2A_B_IO10_P	GND	HSIO_2A_B_IO21_P
49	HSIO_2A_B_IO12_N	GND	HSIO_2A_B_IO19_N	GND
50	HSIO_2A_B_IO12_P	HSIO_2A_B_IO9_N	HSIO_2A_B_IO19_P	HSIO_2A_B_IO20_N
51	GND	HSIO_2A_B_IO9_P	GND	HSIO_2A_B_IO20_P
52	SDM_CONF_DONE_1V8	GND	SDM_TEMPDIODE0A_N	GND
53	SDM_INIT_DONE_1V8	SDM_VSIG0_N	SDM_TEMPDIODE0A_P	SOM_VOUT_1V2
54	SDM_MSEL2_1V8	SDM_VSIG0_P	SDM_VREF_ADC_N	SOM_VOUT_1V2
55	SDM_MSEL1_1V8	SDM_VSIG1_N	SDM_VREF_ADC_P	SOM_VOUT_3V3
56	GND	SDM_VSIG1_P	GND	SOM_VOUT_3V3
57	SDM_JTAG_TMS_1V8	GND	RESERVED	GND
58	SDM_JTAG_TCK_1V8	RESERVED	SDM_HPS_COLD_RESET_B_1V8	SDM_IO11_1V8
59	SDM_JTAG_TDI_1V8	SDM_IO12_1V8	SDM_NCONFIG_1V8	SDM_IO8_1V8
60	SDM_JTAG_TDO_1V8	SDM_IO14_1V8	SDM_NSTATUS_1V8	SDM_IO13_1V8

2.11.2. **CN1 Signal List and Description**

Table 2-11 CN1 Signal List

Pin No.	CN1 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
A1	HSIO_3A_T_IO22_N	IOB,DIFF_IO_3A_T22N	E5	I/O, RX/TX channel	HSIO bank 3A_T IO22 differential (N) / single-ended
A2	HSIO_3A_T_IO22_P	IOB,DIFF_IO_3A_T22P	D5	I/O, RX/TX channel	HSIO bank 3A_T IO22 differential (P) / single-ended
A3	GND				Ground
A4	HSIO_3A_T_IO18_CLK1_N	IOB,DIFF_IO_3A_T18N, CLK_T_3A_1N	E1	I/O, RX/TX channel, Clock Input	HSIO bank 3A_T differential I/O (N) / single-ended I/O / CLK1 differential clock (N) / single-ended clock
A5	HSIO_3A_T_IO18_CLK1_P	IOB,DIFF_IO_3A_T18P, CLK_T_3A_1P	F2	I/O, RX/TX channel, Clock Input	HSIO bank 3A_T differential I/O (P) / single-ended I/O / CLK1 differential clock (P) / single-ended clock
A6	GND				Ground
A7	HSIO_3A_T_IO17_N	IOB,DIFF_IO_3A_T17N	F1	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (N) / single-ended I/O
A8	HSIO_3A_T_IO17_P	IOB,DIFF_IO_3A_T17P	G1	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (P) / single-ended I/O
A9	GND				Ground
A10	RESERVED				Internally unconnected reserved pin
A11	RESERVED				Internally unconnected reserved pin
A12	GND				Ground
A13	HSIO_2A_T_IO1_N	IOB,DIFF_IO_2A_T1N	P7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
A14	HSIO_2A_T_IO1_P	IOB,DIFF_IO_2A_T1P	R7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
A15	GND				Ground
A16	HSIO_2A_T_IO4_N	IOB,DIFF_IO_2A_T4N	R6	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
A17	HSIO_2A_T_IO4_P	IOB,DIFF_IO_2A_T4P	R5	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
A18	GND				Ground
A19	HSIO_2A_T_IO3_N	IOB,DIFF_IO_2A_T3N	T7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
A20	HSIO_2A_T_IO3_P	IOB,DIFF_IO_2A_T3P	T6	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
A21	GND				Ground
A22	HSIO_2A_T_IO5_N	IOB,DIFF_IO_2A_T5N	U6	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
A23	HSIO_2A_T_IO5_P	IOB,DIFF_IO_2A_T5P	V5	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
A24	GND				Ground
A25	HSIO_2A_T_IO15_N	IOB,DIFF_IO_2A_T15N	AA7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
A26	HSIO_2A_T_IO15_P	IOB,DIFF_IO_2A_T15P	AA6	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
A27	GND				Ground
A28	HSIO_2A_T_IO17_N	IOB,DIFF_IO_2A_T17N	AD7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
A29	HSIO_2A_T_IO17_P	IOB,DIFF_IO_2A_T17P	AC7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
A30	GND				Ground
A31	HSIO_2A_T_VCCIO	VCCIO_PIO_2A_T	AC12	Power, Input	HSIO bank 2A_T VCCIO supply voltage (1.0-1.3V)
A32	HSIO_2A_T_VCCIO	VCCIO_PIO_2A_T	AD11	Power, Input	HSIO bank 2A_T VCCIO supply voltage (1.0-1.3V)
A33	GND				Ground
A34	HSIO_2A_B_IO4_N	IOB,DIFF_IO_2A_B4N	AC3	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
A35	HSIO_2A_B_IO4_P	IOB,DIFF_IO_2A_B4P	AB4	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
A36	GND				Ground
A37	HSIO_2A_B_IO6_CLK1_N	IOB,DIFF_IO_2A_B6N, CLK_B_2A_1N	AE5	I/O, RX/TX channel, Clock Input	HSIO bank 2A_B differential I/O (N) / single-ended I/O / CLK1 differential clock (N) / single-ended clock

Pin No.	CN1 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
A38	HSIO_2A_B_IO6_CLK1_P	IOB,DIFF_IO_2A_B6P, CLK_B_2A_1P	AD5	I/O, RX/TX channel, Clock Input	HSIO bank 2A_B differential I/O (P) / single-ended I/O / CLK1 differential clock (P) / single-ended clock
A39	GND				Ground
A40	HSIO_2A_B_IO23_N	IOB,DIFF_IO_2A_B23N	AG3	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
A41	HSIO_2A_B_IO23_P	IOB,DIFF_IO_2A_B23P	AH2	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
A42	GND				Ground
A43	HSIO_2A_B_IO8_N	IOB,DIFF_IO_2A_B8N	AG4	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
A44	HSIO_2A_B_IO8_P	IOB,DIFF_IO_2A_B8P	AF4	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
A45	GND				Ground
A46	HSIO_2A_B_IO11_N	IOB,DIFF_IO_2A_B11N	AE6	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
A47	HSIO_2A_B_IO11_P	IOB,DIFF_IO_2A_B11P	AF6	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
A48	GND				Ground
A49	HSIO_2A_B_IO12_N	IOB,DIFF_IO_2A_B12N	AE7	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
A50	HSIO_2A_B_IO12_P	IOB,DIFF_IO_2A_B12P	AF7	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
A51	GND				Ground
A52	SDM_CONF_DONE_1V8	SDM_IO16	AF9	Output	SDM_IO16 / CONF_DONE
A53	SDM_INIT_DONE_1V8	SDM_IO0	AG10	Output	SDM_IO0 / INIT_DONE
A54	SDM_MSEL2_1V8	SDM_IO9	AJ9	Input	SDM_IO9 / MSEL2
A55	SDM_MSEL1_1V8	SDM_IO7	AK10	Input	SDM_IO7 / MSEL1
A56	GND				Ground
A57	SDM_JTAG_TMS_1V8	TMS	AF17	Input	JTAG test mode select
A58	SDM_JTAG_TCK_1V8	TCK	AF16	Input	JTAG test clock
A59	SDM_JTAG_TDI_1V8	TDI	AE17	Input	JTAG test date input
A60	SDM_JTAG_TDO_1V8	TDO	AE16	Output	JTAG test data output
B1	GND				Ground
B2	HSIO_3A_T_IO23_N	IOB,DIFF_IO_3A_T23N	E6	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (N) / single-ended I/O
B3	HSIO_3A_T_IO23_P	IOB,DIFF_IO_3A_T23P	F6	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (P) / single-ended I/O
B4	GND				Ground
B5	HSIO_3A_T_IO21_N	IOB,DIFF_IO_3A_T21N	E4	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (N) / single-ended I/O
B6	HSIO_3A_T_IO21_P	IOB,DIFF_IO_3A_T21P	F4	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (P) / single-ended I/O
B7	GND				Ground
B8	HSIO_3A_T_IO20_N	IOB,DIFF_IO_3A_T20N	F3	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (N) / single-ended I/O
B9	HSIO_3A_T_IO20_P	IOB,DIFF_IO_3A_T20P	G3	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (P) / single-ended I/O
B10	GND				Ground
B11	RESERVED				Internally unconnected reserved pin
B12	RESERVED				Internally unconnected reserved pin
B13	GND				Ground
B14	HSIO_2A_T_IO2_N	IOB,DIFF_IO_2A_T2N	N7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
B15	HSIO_2A_T_IO2_P	IOB,DIFF_IO_2A_T2P	N6	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
B16	GND				Ground
B17	HSIO_2A_T_IO8_N	IOB,DIFF_IO_2A_T8N	P4	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
B18	HSIO_2A_T_IO8_P	IOB,DIFF_IO_2A_T8P	P5	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
B19	GND				Ground
B20	HSIO_2A_T_IO10_N	IOB,DIFF_IO_2A_T10N	T4	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
B21	HSIO_2A_T_IO10_P	IOB,DIFF_IO_2A_T10P	U5	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
B22	GND				Ground

Pin No.	CN1 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
B23	HSIO_2A_T_IO16_N	IOB,DIFF_IO_2A_T16N	AB6	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
B24	HSIO_2A_T_IO16_P	IOB,DIFF_IO_2A_T16P	AB5	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
B25	GND				Ground
B26	HSIO_2A_T_IO13_N	IOB,DIFF_IO_2A_T13N	W7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
B27	HSIO_2A_T_IO13_P	IOB,DIFF_IO_2A_T13P	V7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
B28	GND				Ground
B29	HSIO_2A_T_IO18_CLK1_N	IOB,DIFF_IO_2A_T18N, CLK_T_2A_1N	AC5	I/O, RX/TX channel, Clock Input	HSIO bank 2A_T differential I/O (N) / single-ended I/O / CLK1 differential clock (N) / single-ended clock
B30	HSIO_2A_T_IO18_CLK1_P	IOB,DIFF_IO_2A_T18P, CLK_T_2A_1P	AC6	I/O, RX/TX channel, Clock Input	HSIO bank 2A_T differential I/O (P) / single-ended I/O / CLK1 differential clock (P) / single-ended clock
B31	GND				Ground
B32	SOM_VOUT_0V9			Power, Output	0.9 V power output (supplied from on-board LDO)
B33	SOM_VOUT_0V9			Power, Output	0.9 V power output (supplied from on-board LDO)
B34	GND				Ground
B35	HSIO_2A_B_IO1_N	IOB,DIFF_IO_2A_B1N	Y5	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
B36	HSIO_2A_B_IO1_P	IOB,DIFF_IO_2A_B1P	W4	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
B37	GND				Ground
B38	HSIO_2A_B_IO5_N	IOB,DIFF_IO_2A_B5N	AD4	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
B39	HSIO_2A_B_IO5_P	IOB,DIFF_IO_2A_B5P	AD3	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
B40	GND				Ground
B41	HSIO_2A_B_IO7_CLK0_N	IOB,DIFF_IO_2A_B7N, CLK_B_2A_0N	AE4	I/O, RX/TX channel, Clock Input	HSIO bank 2A_B differential I/O (N) / single-ended I/O / CLK1 differential clock (N) / single-ended clock
B42	HSIO_2A_B_IO7_CLK0_P	IOB,DIFF_IO_2A_B7P, CLK_B_2A_0P	AF3	I/O, RX/TX channel, Clock Input	HSIO bank 2A_B differential I/O (P) / single-ended I/O / CLK1 differential clock (P) / single-ended clock
B43	GND				Ground
B44	HSIO_2A_B_IO24_N	IOB,DIFF_IO_2A_B24N	AH3	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
B45	HSIO_2A_B_IO24_P	IOB,DIFF_IO_2A_B24P	AJ3	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
B46	GND				Ground
B47	HSIO_2A_B_IO10_N	IOB,DIFF_IO_2A_B10N	AG5	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
B48	HSIO_2A_B_IO10_P	IOB,DIFF_IO_2A_B10P	AH5	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
B49	GND				Ground
B50	HSIO_2A_B_IO9_N	IOB,DIFF_IO_2A_B9N	AG6	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
B51	HSIO_2A_B_IO9_P	IOB,DIFF_IO_2A_B9P	AH6	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
B52	GND				Ground
B53	SDM_VSIG0_N	VSIGN_0	AJ14	Input	Analog input channel 0 (N) of internal voltage sensor
B54	SDM_VSIG0_P	VSIGP_0	AK14	Input	Analog input channel 0 (P) of internal voltage sensor
B55	SDM_VSIG1_N	VSIGN_1	AK16	Input	Analog input channel 1 (N) of internal voltage sensor
B56	SDM_VSIG1_P	VSIGP_1	AK17	Input	Analog input channel 1 (P) of internal voltage sensor
B57	GND				Ground
B58	RESERVED				Internally unconnected reserved pin
B59	SDM_IO12_1V8	SDM_IO12	AF11	Input, Output	SDM_IO12
B60	SDM_IO14_1V8	SDM_IO14	AJ10	Input, Output	SDM_IO14

Pin No.	CN1 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
C1	HSIO_3A_T_IO24_N	IOB,DIFF_IO_3A_T24N	D4	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (N) / single-ended I/O
C2	HSIO_3A_T_IO24_P	IOB,DIFF_IO_3A_T24P	C5	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (P) / single-ended I/O
C3	GND				Ground
C4	HSIO_3A_T_IO16_N	IOB,DIFF_IO_3A_T16N	H1	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (N) / single-ended I/O
C5	HSIO_3A_T_IO16_P	IOB,DIFF_IO_3A_T16P	H2	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (P) / single-ended I/O
C6	GND				Ground
C7	HSIO_3A_T_IO15_N	IOB,DIFF_IO_3A_T15N	K2	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (N) / single-ended I/O
C8	HSIO_3A_T_IO15_P	IOB,DIFF_IO_3A_T15P	J2	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (P) / single-ended I/O
C9	GND				Ground
C10	RESERVED				Internally unconnected reserved pin
C11	RESERVED				Internally unconnected reserved pin
C12	GND				Ground
C13	HSIO_2A_T_IO7_N	IOB,DIFF_IO_2A_T7N	P3	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
C14	HSIO_2A_T_IO7_P	IOB,DIFF_IO_2A_T7P	N3	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
C15	GND				Ground
C16	HSIO_2A_T_IO9_N	IOB,DIFF_IO_2A_T9N	R4	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
C17	HSIO_2A_T_IO9_P	IOB,DIFF_IO_2A_T9P	T3	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
C18	GND				Ground
C19	HSIO_2A_T_IO11_N	IOB,DIFF_IO_2A_T11N	U3	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
C20	HSIO_2A_T_IO11_P	IOB,DIFF_IO_2A_T11P	U4	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
C21	GND				Ground
C22	HSIO_2A_T_IO12_N	IOB,DIFF_IO_2A_T12N	W3	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
C23	HSIO_2A_T_IO12_P	IOB,DIFF_IO_2A_T12P	V3	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
C24	GND				Ground
C25	HSIO_2A_T_IO6_N	IOB,DIFF_IO_2A_T6N	W5	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
C26	HSIO_2A_T_IO6_P	IOB,DIFF_IO_2A_T6P	V6	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
C27	GND				Ground
C28	HSIO_2A_T_IO14_N	IOB,DIFF_IO_2A_T14N	Y6	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
C29	HSIO_2A_T_IO14_P	IOB,DIFF_IO_2A_T14P	Y7	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
C30	GND				Ground
C31	RESERVED				Internally unconnected reserved pin
C32	RESERVED				Internally unconnected reserved pin
C33	GND				Ground
C34	HSIO_2A_B_IO2_N	IOB,DIFF_IO_2A_B2N	AA3	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
C35	HSIO_2A_B_IO2_P	IOB,DIFF_IO_2A_B2P	Y4	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
C36	GND				Ground
C37	HSIO_2A_B_IO3_N	IOB,DIFF_IO_2A_B3N	AA4	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
C38	HSIO_2A_B_IO3_P	IOB,DIFF_IO_2A_B3P	AB3	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
C39	GND				Ground
C40	HSIO_2A_B_IO16_N	IOB,DIFF_IO_2A_B16N	AC2	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
C41	HSIO_2A_B_IO16_P	IOB,DIFF_IO_2A_B16P	AC1	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
C42	GND				Ground
C43	HSIO_2A_B_IO14_N	IOB,DIFF_IO_2A_B14N	AE2	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O

Pin No.	CN1 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
C44	HSIO_2A_B_IO14_P	IOB,DIFF_IO_2A_B14P	AF1	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
C45	GND				Ground
C46	HSIO_2A_B_IO22_N	IOB,DIFF_IO_2A_B22N	AJ4	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
C47	HSIO_2A_B_IO22_P	IOB,DIFF_IO_2A_B22P	AK4	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
C48	GND				Ground
C49	HSIO_2A_B_IO19_N	IOB,DIFF_IO_2A_B19N	AJ7	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
C50	HSIO_2A_B_IO19_P	IOB,DIFF_IO_2A_B19P	AK6	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
C51	GND				Ground
C52	SDM_TEMPDIODE0A_N	TEMPDIODE0AN	AH17	Input	Internal temperature-sensing diode (N)
C53	SDM_TEMPDIODE0A_P	TEMPDIODE0AP	AH16	Input	Internal temperature-sensing diode (P)
C54	SDM_VREF_ADC_N	VREFN_ADC	AK15	Input	External reference for internal ADC (N)
C55	SDM_VREF_ADC_P	VREFP_ADC	AJ15	Input	External reference for internal ADC (P)
C56	GND				Ground
C57	RESERVED				Internally unconnected reserved pin
C58	SDM_HPS_COLD_RESET_B_1V8	SDM_IO10	AH11	Input	SDM_IO10 / HPS_COLD_nRESET
C59	SDM_NCONFIG_1V8	NCONFIG	AG15	Input	nCONFIG
C60	SDM_NSTATUS_1V8	NSTATUS	AG16	Input	nSTATUS
D1	GND				Ground
D2	HSIO_3A_T_IO19_CLK0_N	IOB,DIFF_IO_3A_T19N, CLK_T_3A_1N	E2	I/O, RX/TX channel, Clock Input	HSIO bank 3A_T differential I/O (N) / single-ended I/O / CLK0 differential clock (N) / single-ended clock
D3	HSIO_3A_T_IO19_CLK0_P	IOB,DIFF_IO_3A_T19P, CLK_T_3A_1P	D2	I/O, RX/TX channel, Clock Input	HSIO bank 3A_T differential I/O (P) / single-ended I/O / CLK0 differential clock (P) / single-ended clock
D4	GND				Ground
D5	HSIO_3A_T_IO14_N	IOB,DIFF_IO_3A_T14N	K1	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (N) / single-ended I/O
D6	HSIO_3A_T_IO14_P	IOB,DIFF_IO_3A_T14P	L2	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (P) / single-ended I/O
D7	GND				Ground
D8	HSIO_3A_T_IO13_N	IOB,DIFF_IO_3A_T13N	L1	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (N) / single-ended I/O
D9	HSIO_3A_T_IO13_P	IOB,DIFF_IO_3A_T13P	M1	I/O, RX/TX channel	HSIO bank 3A_T differential I/O (P) / single-ended I/O
D10	GND				Ground
D11	SOM_VOUT_1V1			Power, Output	1.1 V power output (supplied from on-board DC/DC)
D12	SOM_VOUT_1V1			Power, Output	1.1 V power output (supplied from on-board DC/DC)
D13	GND				Ground
D14	HSIO_2A_T_IO19_CLK0_N	IOB,DIFF_IO_2A_T19N, CLK_T_2A_0N	N1	I/O, RX/TX channel, Clock Input	HSIO bank 2A_T differential I/O (N) / single-ended I/O / CLK0 differential clock (N) / single-ended clock
D15	HSIO_2A_T_IO19_CLK0_P	IOB,DIFF_IO_2A_T19P, CLK_T_2A_0P	N2	I/O, RX/TX channel, Clock Input	HSIO bank 2A_T differential I/O (P) / single-ended I/O / CLK0 differential clock (P) / single-ended clock
D16	GND				Ground
D17	HSIO_2A_T_IO20_N	IOB,DIFF_IO_2A_T20N	P2	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
D18	HSIO_2A_T_IO20_P	IOB,DIFF_IO_2A_T20P	R1	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
D19	GND				Ground
D20	HSIO_2A_T_IO21_N	IOB,DIFF_IO_2A_T21N	T1	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
D21	HSIO_2A_T_IO21_P	IOB,DIFF_IO_2A_T21P	R2	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
D22	GND				Ground
D23	HSIO_2A_T_IO22_N	IOB,DIFF_IO_2A_T22N	U1	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O

Pin No.	CN1 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
D24	HSIO_2A_T_IO22_P	IOB,DIFF_IO_2A_T22P	T2	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
D25	GND				Ground
D26	HSIO_2A_T_IO23_N	IOB,DIFF_IO_2A_T23N	V2	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
D27	HSIO_2A_T_IO23_P	IOB,DIFF_IO_2A_T23P	V1	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
D28	GND				Ground
D29	HSIO_2A_T_IO24_N	IOB,DIFF_IO_2A_T24N	W2	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (N) / single-ended I/O
D30	HSIO_2A_T_IO24_P	IOB,DIFF_IO_2A_T24P	Y1	I/O, RX/TX channel	HSIO bank 2A_T differential I/O (P) / single-ended I/O
D31	GND				Ground
D32	HSIO_2A_B_VCCIO	VCCIO_PIO_2A_B	AC14	Power, Input	HSIO bank 2A_B VCCIO supply voltage (1.0-1.3V)
D33	HSIO_2A_B_VCCIO	VCCIO_PIO_2A_B	AD13	Power, Input	HSIO bank 2A_B VCCIO supply voltage (1.0-1.3V)
D34	GND				Ground
D35	HSIO_2A_B_IO17_N	IOB,DIFF_IO_2A_B17N	AA1	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
D36	HSIO_2A_B_IO17_P	IOB,DIFF_IO_2A_B17P	Y2	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
D37	GND				Ground
D38	HSIO_2A_B_IO18_N	IOB,DIFF_IO_2A_B18N	AA2	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
D39	HSIO_2A_B_IO18_P	IOB,DIFF_IO_2A_B18P	AB1	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
D40	GND				Ground
D41	HSIO_2A_B_IO15_N	IOB,DIFF_IO_2A_B15N	AE1	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
D42	HSIO_2A_B_IO15_P	IOB,DIFF_IO_2A_B15P	AD2	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
D43	GND				Ground
D44	HSIO_2A_B_IO13_N	IOB,DIFF_IO_2A_B13N	AF2	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
D45	HSIO_2A_B_IO13_P	IOB,DIFF_IO_2A_B13P	AG1	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
D46	GND				Ground
D47	HSIO_2A_B_IO21_N	IOB,DIFF_IO_2A_B21N	AK5	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
D48	HSIO_2A_B_IO21_P	IOB,DIFF_IO_2A_B21P	AJ5	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
D49	GND				Ground
D50	HSIO_2A_B_IO20_N	IOB,DIFF_IO_2A_B20N	AJ8	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (N) / single-ended I/O
D51	HSIO_2A_B_IO20_P	IOB,DIFF_IO_2A_B20P	AK7	I/O, RX/TX channel	HSIO bank 2A_B differential I/O (P) / single-ended I/O
D52	GND				Ground
D53	SOM_VOUT_1V2			Power, Output	1.2 V power output (supplied from on-board DC/DC)
D54	SOM_VOUT_1V2			Power, Output	1.2 V power output (supplied from on-board DC/DC)
D55	SOM_VOUT_3V3			Power, Output	3.3 V power output (supplied from on-board DC/DC)
D56	SOM_VOUT_3V3			Power, Output	3.3 V power output (supplied from on-board DC/DC)
D57	GND				Ground
D58	SDM_IO11_1V8	SDM_IO11	AG9	Input, Output	SDM_IO11
D59	SDM_IO8_1V8	SDM_IO8	AF13	Input, Output	SDM_IO8
D60	SDM_IO13_1V8	SDM_IO13	AF12	Input, Output	SDM_IO13

2.12. **Board-to-Board Connector 2 (CN2)**

The layout, pin assignment, and pin description of Board-to-Board Connector 2 are shown below.

Connector part number: ADF6-60-03.5-L-4-2-A-TR (Samtec)

Mating connector part number: ADM6-60-01.5-L-4-2-A-TR (Samtec)

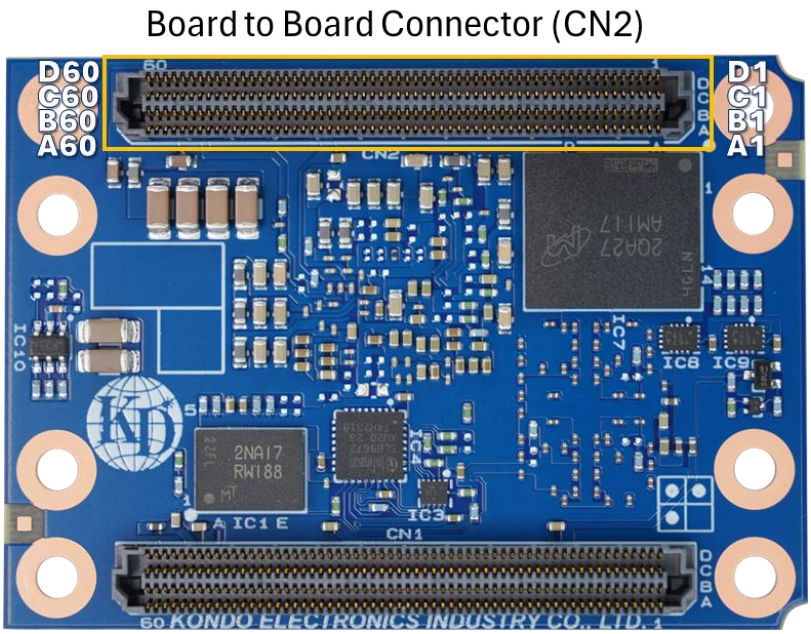


Figure 2-13 Board-to-Board Connector 2 Layout

2.12.1. **CN2 Pin Assignment**

Table 2-12 CN2 Pin Assignment

Pin No.	A Row	B Row	C Row	D Row
1	GND	HPS_SDMMC_DATA3_1V8	GND	HPS_RGMII_RXD3_1V8
2	HPS_IOB12_1V8	HPS_SDMMC_DATA2_1V8	HPS_RGMII_TX_CLK_1V8	HPS_RGMII_RXD0_1V8
3	HPS_IOB9_1V8	HPS_SDMMC_DATA0_1V8	HPS_RGMII_TX_CTRL_1V8	HPS_RGMII_RXD2_1V8
4	HPS_IOB10_1V8	HPS_SDMMC_DATA1_1V8	HPS_RGMII_TXD1_1V8	HPS_RGMII_RXD1_1V8
5	HPS_IOB11_1V8	GND	HPS_RGMII_TXD3_1V8	GND
6	GND	HPS_SDMMC_CMD_1V8	GND	HPS_RGMII_RX_CTRL_1V8
7	HPS_IOB5_1V8	HPS_SDMMC_CLK_1V8	HPS_RGMII_TXD2_1V8	HPS_RGMII_RX_CLK_1V8
8	HPS_ULPI_NXT_1V8	HPS_ULPI_DATA0_1V8	HPS_RGMII_TXD0_1V8	HPS_I2C_SCL_1V8
9	HPS_ULPI_DATA5_1V8	HPS_ULPI_DATA1_1V8	HPS_ETH_MDIO_1V8	HPS_I2C_SDA_1V8
10	HPS_ULPI_DATA3_1V8	GND	HPS_ETH_MDC_1V8	GND
11	GND	HPS_ULPI_DATA2_1V8	GND	HPS_IOA12_1V8
12	HPS_ULPI_DATA7_1V8	HPS_ULPI_DATA4_1V8	HPS_ETH_INT_B_1V8	HPS_IOA11_1V8
13	HPS_ULPI_DATA6_1V8	HPS_ULPI_CLK_1V8	HPS_IOA1_1V8	HPS_1PPS_IN_1V8
14	HPS_ULPI_STP_1V8	HPS_OSC_CLK_1V8	HPS_UART_RXD_1V8	HPS_1PPS_OUT_1V8
15	HPS_ULPI_DIR_1V8	RESERVED	HPS_UART_TXD_1V8	RESERVED
16	RESERVED	GND	RESERVED	GND
17	GND	GTSL_1A_CDRCLKOUT_CH2_N	GND	RESERVED
18	GND	GTSL_1A_CDRCLKOUT_CH2_P	GND	RESERVED
19	GTSL_1A_TX_CH3_N	GND	GTSL_1A_TX_CH2_N	GND
20	GTSL_1A_TX_CH3_P	GND	GTSL_1A_TX_CH2_P	GND

Pin No.	A Row	B Row	C Row	D Row
21	GND	GTSL_1A_RX_CH3_N	GND	GTSL_1A_RX_CH2_N
22	GND	GTSL_1A_RX_CH3_P	GND	GTSL_1A_RX_CH2_P
23	GTSL_1A_TX_CH1_N	GND	GTSL_1A_TX_CH0_N	GND
24	GTSL_1A_TX_CH1_P	GND	GTSL_1A_TX_CH0_P	GND
25	GND	GTSL_1A_RX_CH1_N	GND	GTSL_1A_RX_CH0_N
26	GND	GTSL_1A_RX_CH1_P	GND	GTSL_1A_RX_CH0_P
27	GTSL_1A_REFCLK_CH1_N	GND	GTSL_1A_REFCLK_RX_N	GND
28	GTSL_1A_REFCLK_CH1_P	GND	GTSL_1A_REFCLK_RX_P	GND
29	GND	GTSL_1X_TX_CH3_N	GND	GTSL_1X_TX_CH2_N
30	GND	GTSL_1X_TX_CH3_P	GND	GTSL_1X_TX_CH2_P
31	GTSL_1X_RX_CH3_N	GND	GTSL_1X_RX_CH2_N	GND
32	GTSL_1X_RX_CH3_P	GND	GTSL_1X_RX_CH2_P	GND
33	GND	GTSL_1X_TX_CH1_N	GND	GTSL_1X_TX_CH0_N
34	GND	GTSL_1X_TX_CH1_P	GND	GTSL_1X_TX_CH0_P
35	GTSL_1X_RX_CH1_N	GND	GTSL_1X_RX_CH0_N	GND
36	GTSL_1X_RX_CH1_P	GND	GTSL_1X_RX_CH0_P	GND
37	GND	GTSL_1X_REFCLK_CH1_N	GND	GTSL_1X_REFCLK_RX_N
38	GND	GTSL_1X_REFCLK_CH1_P	GND	GTSL_1X_REFCLK_RX_P
39	HVIO_5A_VCCIO	GND	HVIO_5B_VCCIO	GND
40	HVIO_5A_VCCIO	RESERVED	HVIO_5B_VCCIO	RESERVED
41	HVIO_5A_IO15	RESERVED	HVIO_5B_IO15	RESERVED
42	HVIO_5A_IO13	HVIO_5A_IO14	HVIO_5B_IO17	HVIO_5B_IO13
43	GND	HVIO_5A_IO18	GND	HVIO_5B_IO18
44	HVIO_5A_IO7	GND	HVIO_5B_IO20	GND
45	HVIO_5A_IO5	HVIO_5A_IO2	HVIO_5B_IO10	HVIO_5B_IO9
46	HVIO_5A_IO6	HVIO_5A_IO1	HVIO_5B_IO7	HVIO_5B_IO14
47	HVIO_5A_IO9	HVIO_5A_IO12	HVIO_5B_IO2	HVIO_5B_IO3
48	GND	HVIO_5A_IO3	GND	HVIO_5B_IO1
49	HVIO_5A_IO10	GND	HVIO_5B_IO5	GND
50	HVIO_5A_IO8	HVIO_5A_IO16	HVIO_5B_IO4	HVIO_5B_IO12
51	HVIO_5A_IO11	HVIO_5A_IO4	HVIO_5B_IO6	HVIO_5B_IO8
52	HVIO_5A_IO17	HVIO_5A_IO20	HVIO_5B_IO19	HVIO_5B_IO16
53	GND	HVIO_5A_IO19	GND	HVIO_5B_IO11
54	1.8V_VCCBAT	GND	SOM_PWR_OK_3V3	GND
55	RESERVED	SOM_EMMC_RST_B_1V8	SOM_PWR_EN_3V3	RESERVED
56	GND	SOM_SDMMC_SEL_1V8	GND	RESERVED
57	GND	GND	GND	GND
58	SOM_VIN	SOM_VIN	SOM_VIN	SOM_VIN
59	SOM_VIN	SOM_VIN	SOM_VIN	SOM_VIN
60	SOM_VIN	SOM_VIN	SOM_VIN	SOM_VIN

2.12.2. **CN2 Signal List and Description**

Table 2-13 CN2 Signal List

Pin No.	CN2 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
A1	GND				Ground
A2	HPS_IOB12_1V8	HPS_IOB_12	A22	I/O	HPS IOB bit 12
A3	HPS_IOB9_1V8	HPS_IOB_9	C22	I/O	HPS IOB bit 9
A4	HPS_IOB10_1V8	HPS_IOB_10	D19	I/O	HPS IOB bit 10
A5	HPS_IOB11_1V8	HPS_IOB_11	B21	I/O	HPS IOB bit 11
A6	GND				Ground
A7	HPS_IOB5_1V8	HPS_IOB_5	A17	I/O	HPS IOB bit 5
A8	HPS_ULPI_NXT_1V8	HPS_IOA_18 / USB1_NXT	E16	I/O, Input	HPS IOA bit 18 / USB1 Next signal
A9	HPS_ULPI_DATA5_1V8	HPS_IOA_22 / USB1_DATA5	D20	I/O	HPS IOA bit 22 / USB1 Data bit 5
A10	HPS_ULPI_DATA3_1V8	HPS_IOA_20 / USB1_DATA3	E21	I/O	HPS IOA bit 20 / USB1 Data bit 3
A11	GND				Ground
A12	HPS_ULPI_DATA7_1V8	HPS_IOA_24 / USB1_DATA7	A24	I/O	HPS IOA bit 24 / USB1 Data bit 7
A13	HPS_ULPI_DATA6_1V8	HPS_IOA_23 / USB1_DATA6	B24	I/O	HPS IOA bit 23 / USB1 Data bit 6
A14	HPS_ULPI_STP_1V8	HPS_IOA_14 / USB1_STP	B26	I/O, Output	HPS IOA bit 14 / USB1 Stop signal
A15	HPS_ULPI_DIR_1V8	HPS_IOA_15 / USB1_DIR	B25	I/O, Input	HPS IOA bit 15 / USB1 Direction
A16	RESERVED				Internally unconnected reserved pin
A17	GND				Ground
A18	GND				Ground
A19	GTSL_1A_TX_CH3_N	GTSL1A_TX_CH3N / GTSL1B_TX_CH3N	F27	Output	Non-028B models: Transceiver bank 1A Transmit Channel 3 (N) 028B model: Transceiver bank 1B Transceiver Channel 3 (N)
A20	GTSL_1A_TX_CH3_P	GTSL1A_TX_CH3P / GTSL1B_TX_CH3P	G27	Output	Non-028B models: Transceiver bank 1A Transmit Channel 3 (P) 028B model: Transceiver bank 1B Transceiver Channel 3 (P)
A21	GND				Ground
A22	GND				Ground
A23	GTSL_1A_TX_CH1_N	GTSL1A_TX_CH1N / GTSL1B_TX_CH1N	M28	Output	Non-028B models: Transceiver bank 1A Transmit Channel 1 (N) 028B model: Transceiver bank 1B Transceiver Channel 1 (N)
A24	GTSL_1A_TX_CH1_P	GTSL1A_TX_CH1P / GTSL1B_TX_CH1P	M29	Output	Non-028B models: Transceiver bank 1A Transmit Channel 1 (P) 028B model: Transceiver bank 1B Transceiver Channel 1 (P)
A25	GND				Ground
A26	GND				Ground
A27	GTSL_1A_REFCLK_CH1_N	REFCLK_GTSL1A_CH1N / REFCLK_GTSL1B_CH1N	M25	Input	Non-028B models: Transceiver bank 1A Local Reference Clock (N) 028B model: Transceiver bank 1B Local Reference Clock (N)
A28	GTSL_1A_REFCLK_CH1_P	REFCLK_GTSL1A_CH1P / REFCLK_GTSL1B_CH1P	M24	Input	Non-028B models: Transceiver bank 1A Local Reference Clock (P) 028B model: Transceiver bank 1B Local Reference Clock (P)
A29	GND				Ground
A30	GND				Ground
A31	GTSL_1X_RX_CH3_N	NC / GTSL1A_RX_CH3N	Y30	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Receive Channel 3 (N)
A32	GTSL_1X_RX_CH3_P	NC / GTSL1A_RX_CH3P	Y29	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Receive Channel 3 (P)
A33	GND				Ground
A34	GND				Ground
A35	GTSL_1X_RX_CH1_N	NC / GTSL1A_RX_CH1N	AD30	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Receive Channel 1 (N)

Pin No.	CN2 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
A36	GTSL_1X_RX_CH1_P	NC / GTSL1A_RX_CH1P	AD29	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Receive Channel 1 (P)
A37	GND				Ground
A38	GND				Ground
A39	HVIO_5A_VCCIO	VCCIO_HVIO_5A	AD22	Power, Input	HVIO bank 5A VCCIO supply voltage (1.8-3.3V)
A40	HVIO_5A_VCCIO	VCCIO_HVIO_5A	AE21	Power, Input	HVIO bank 5A VCCIO supply voltage (1.8-3.3V)
A41	HVIO_5A_IO15	HVIO_5A_15	AF23	I/O	HVIO bank 5A single-ended I/O
A42	HVIO_5A_IO13	HVIO_5A_13	AF24	I/O	HVIO bank 5A single-ended I/O
A43	GND				Ground
A44	HVIO_5A_IO7	HVIO_5A_7	AG23	I/O	HVIO bank 5A single-ended I/O
A45	HVIO_5A_IO5	HVIO_5A_5	AH23	I/O	HVIO bank 5A single-ended I/O
A46	HVIO_5A_IO6	HVIO_5A_6	AH22	I/O	HVIO bank 5A single-ended I/O
A47	HVIO_5A_IO9	HVIO_5A_9	AJ22	I/O	HVIO bank 5A single-ended I/O
A48	GND				Ground
A49	HVIO_5A_IO10	HVIO_5A_10	AJ20	I/O	HVIO bank 5A single-ended I/O
A50	HVIO_5A_IO8	HVIO_5A_8	AH20	I/O	HVIO bank 5A single-ended I/O
A51	HVIO_5A_IO11	HVIO_5A_11	AH18	I/O	HVIO bank 5A single-ended I/O
A52	HVIO_5A_IO17	HVIO_5A_17	AG19	I/O	HVIO bank 5A single-ended I/O
A53	GND				Ground
A54	1.8V_VCCBAT	VCCBAT	AC18	Power, Input	AES BBRAM supply voltage
A55	RESERVED				Internally unconnected reserved pin
A56	GND				Ground
A57	GND				Ground
A58	SOM_VIN			Power, Input	SoM supply voltage
A59	SOM_VIN			Power, Input	SoM supply voltage
A60	SOM_VIN			Power, Input	SoM supply voltage
B1	HPS_SDMMC_DATA3_1V8	HPS_IOB_7 / SDMMC_DATA3	C23	I/O	HPS IOB bit 7 / SDMMC Data 3
B2	HPS_SDMMC_DATA2_1V8	HPS_IOB_6 / SDMMC_DATA2	C21	I/O	HPS IOB bit 6 / SDMMC Data 2
B3	HPS_SDMMC_DATA0_1V8	HPS_IOB_1 / SDMMC_DATA0	D23	I/O	HPS IOB bit 1 / SDMMC Data 0
B4	HPS_SDMMC_DATA1_1V8	HPS_IOB_2 / SDMMC_DATA1	C25	I/O	HPS IOB bit 2 / SDMMC Data 1
B5	GND				Ground
B6	HPS_SDMMC_CMD_1V8	HPS_IOB_8 / SDMMC_CMD	E20	I/O	HPS IOB bit 8 / SDMMC Command
B7	HPS_SDMMC_CLK_1V8	HPS_IOB_3 / SDMMC_CLK	A18	I/O, Output	HPS IOB bit 3 / SDMMC Clock
B8	HPS_ULPI_DATA0_1V8	HPS_IOA_16 / USB1_DATA0	E17	I/O	HPS IOA bit 16 / USB1 Data bit 0
B9	HPS_ULPI_DATA1_1V8	HPS_IOA_17 / USB1_DATA1	A16	I/O	HPS IOA bit 17 / USB1 Data bit 1
B10	GND				Ground
B11	HPS_ULPI_DATA2_1V8	HPS_IOA_19 / USB1_DATA2	D24	I/O	HPS IOA bit 19 / USB1 Data bit 2
B12	HPS_ULPI_DATA4_1V8	HPS_IOA_21 / USB1_DATA4	B23	I/O	HPS IOA bit 21 / USB1 Data bit 4
B13	HPS_ULPI_CLK_1V8	HPS_IOA_13 / USB1_CLK	D25	I/O, Output	HPS IOA bit 13 / USB1 Clock
B14	HPS_OSC_CLK_1V8	HPS_IOB_4 / HPS_OSC_CLK	C20	I/O, Input	HPS IOB bit 4 / Clock Input
B15	RESERVED				Internally unconnected reserved pin
B16	GND				Ground
B17	GTSL_1A_CDRCLKOUT_CH2_N	CDRCLKOUT_GTSL1A_CH2N / CDRCLKOUT_GTSL1B_CH2N	K25	Output	Non-028B models: Transceiver bank 1A CDR Recovery Clock (N) 028B model: Transceiver bank 1B CDR Recovery Clock (N)
B18	GTSL_1A_CDRCLKOUT_CH2_P	CDRCLKOUT_GTSL1A_CH2P / CDRCLKOUT_GTSL1B_CH2P	K24	Output	Non-028B models: Transceiver bank 1A CDR Recovery Clock (P) 028B model: Transceiver bank 1B CDR Recovery Clock (P)

Pin No.	CN2 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
B19	GND				Ground
B20	GND				Ground
B21	GTSL_1A_RX_CH3_N	GTSL1A_RX_CH3N / GTSL1B_RX_CH3N	D29	Input	Non-028B models: Transceiver bank 1A Receive Channel 3 (N) 028B model: Transceiver bank 1B Receive Channel 3 (N)
B22	GTSL_1A_RX_CH3_P	GTSL1A_RX_CH3P / GTSL1B_RX_CH3P	D30	Input	Non-028B models: Transceiver bank 1A Receive Channel 3 (P) 028B model: Transceiver bank 1B Receive Channel 3 (P)
B23	GND				Ground
B24	GND				Ground
B25	GTSL_1A_RX_CH1_N	GTSL1A_RX_CH1N / GTSL1B_RX_CH1N	H29	Input	Non-028B models: Transceiver bank 1A Receive Channel 1 (N) 028B model: Transceiver bank 1B Receive Channel 1 (N)
B26	GTSL_1A_RX_CH1_P	GTSL1A_RX_CH1P / GTSL1B_RX_CH1P	H30	Input	Non-028B models: Transceiver bank 1A Receive Channel 1 (P) 028B model: Transceiver bank 1B Receive Channel 1 (P)
B27	GND				Ground
B28	GND				Ground
B29	GTSL_1X_TX_CH3_N	NC / GTSL1A_TX_CH3N	T29	Output	Non-028B models: Not connected 028B model: Transceiver bank 1A Transmit Channel 3 (N)
B30	GTSL_1X_TX_CH3_P	NC / GTSL1A_TX_CH3P	T30	Output	Non-028B models: Not connected 028B model: Transceiver bank 1A Transmit Channel 3 (P)
B31	GND				Ground
B32	GND				Ground
B33	GTSL_1X_TX_CH1_N	NC / GTSL1A_TX_CH1N	Y27	Output	Non-028B models: Not connected 028B model: Transceiver bank 1A Transmit Channel 1 (N)
B34	GTSL_1X_TX_CH1_P	NC / GTSL1A_TX_CH1P	AA27	Output	Non-028B models: Not connected 028B model: Transceiver bank 1A Transmit Channel 1 (P)
B35	GND				Ground
B36	GND				Ground
B37	GTSL_1X_REFCLK_CH1_N	NC / REFCLK_GTSL1A_CH1N	V25	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Local Reference Clock (N)
B38	GTSL_1X_REFCLK_CH1_P	NC / REFCLK_GTSL1A_CH1P	V24	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Local Reference Clock (P)
B39	GND				Ground
B40	RESERVED				Internally unconnected reserved pin
B41	RESERVED				Internally unconnected reserved pin
B42	HVIO_5A_IO14	HVIO_5A_14	AG24	I/O	HVIO bank 5A single-ended I/O
B43	HVIO_5A_IO18	HVIO_5A_18	AF22	I/O	HVIO bank 5A single-ended I/O
B44	GND				Ground
B45	HVIO_5A_IO2	HVIO_5A_2	AJ23	I/O	HVIO bank 5A single-ended I/O
B46	HVIO_5A_IO1	HVIO_5A_1	AJ24	I/O	HVIO bank 5A single-ended I/O
B47	HVIO_5A_IO12	HVIO_5A_12	AG21	I/O	HVIO bank 5A single-ended I/O
B48	HVIO_5A_IO3	HVIO_5A_3	AH21	I/O	HVIO bank 5A single-ended I/O
B49	GND				Ground
B50	HVIO_5A_IO16	HVIO_5A_16	AG20	I/O	HVIO bank 5A single-ended I/O
B51	HVIO_5A_IO4	HVIO_5A_4	AJ19	I/O	HVIO bank 5A single-ended I/O
B52	HVIO_5A_IO20	HVIO_5A_20	AF21	I/O	HVIO bank 5A single-ended I/O
B53	HVIO_5A_IO19	HVIO_5A_19	AF19	I/O	HVIO bank 5A single-ended I/O
B54	GND				Ground
B55	SOM_EMMC_RST_B_1V8			Input	eMMC Reset input
B56	SOM_SDMMC_SEL_1V8			Input	SD/eMMC Select Signal. High: eMMC, Low: SD
B57	GND				Ground
B58	SOM_VIN			Power, Input	SoM supply voltage
B59	SOM_VIN			Power, Input	SoM supply voltage

Pin No.	CN2 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
B60	SOM_VIN			Power, Input	SoM supply voltage
C1	GND				Ground
C2	HPS_RGMII_TX_CLK_1V8	HPS_IOB_13 / EMAC2_TX_CLK	B16	I/O, Output	HPS IOB bit 13 / EMAC2 Transmit Clock
C3	HPS_RGMII_TX_CTRL_1V8	HPS_IOB_14 / EMAC2_TX_CTL	B18	I/O, Output	HPS IOB bit 14 / EMAC2 Transmit Control
C4	HPS_RGMII_TXD1_1V8	HPS_IOB_18 / EMAC2_TXD1	A21	I/O, Output	HPS IOB bit 18 / EMAC2 Transmit Data bit 1
C5	HPS_RGMII_TXD3_1V8	HPS_IOB_22 / EMAC2_TXD3	B19	I/O, Output	HPS IOB bit 22 / EMAC2 Transmit Data bit 3
C6	GND				Ground
C7	HPS_RGMII_TXD2_1V8	HPS_IOB_21 / EMAC2_TXD2	D18	I/O, Output	HPS IOB bit 21 / EMAC2 Transmit Data bit 2
C8	HPS_RGMII_TXD0_1V8	HPS_IOB_17 / EMAC2_TXD0	C18	I/O, Output	HPS IOB bit 17 / EMAC2 Transmit Data bit 0
C9	HPS_ETH_MDIO_1V8	HPS_IOA_7 / I2C_EMAC2_SDA	D27	I/O	HPS IOA bit 7 / EMAC2 Serial Data (MDIO)
C10	HPS_ETH_MDC_1V8	HPS_IOA_8 / I2C_EMAC2_SCL	E22	I/O	HPS IOA bit 8 / EMAC2 Serial Clock (MDC)
C11	GND				Ground
C12	HPS_ETH_INT_B_1V8	HPS_IOA_2	A27	I/O, Input	HPS IOA bit 2 / Ethernet Interrupt
C13	HPS_IOA1_1V8	HPS_IOA_1	B29	I/O	HPS IOA bit 1
C14	HPS_UART_RXD_1V8	HPS_IOA_4 / UART0_RX	F24	I/O, Input	HPS IOA bit 4 / UART0 Receive Data
C15	HPS_UART_TXD_1V8	HPS_IOA_3 / UART0_TX	C27	I/O, Output	HPS IOA bit 3 / UART0 Transmit Data
C16	RESERVED				Internally unconnected reserved pin
C17	GND				Ground
C18	GND				Ground
C19	GTSL_1A_TX_CH2_N	GTSL1A_TX_CH2N / GTSL1B_TX_CH2N	J27	Output	Non-028B models: Transceiver bank 1A Transmit Channel 2 (N) 028B model: Transceiver bank 1B Transmit Channel 2 (N)
C20	GTSL_1A_TX_CH2_P	GTSL1A_TX_CH2P / GTSL1B_TX_CH2P	K27	Output	Non-028B models: Transceiver bank 1A Transmit Channel 2 (P) 028B model: Transceiver bank 1B Transmit Channel 2 (P)
C21	GND				Ground
C22	GND				Ground
C23	GTSL_1A_TX_CH0_N	GTSL1A_TX_CH0N / GTSL1B_TX_CH0N	P29	Output	Non-028B models: Transceiver bank 1A Transmit Channel 0 (N) 028B model: Transceiver bank 1B Transmit Channel 0 (N)
C24	GTSL_1A_TX_CH0_P	GTSL1A_TX_CH0P / GTSL1B_TX_CH0P	P30	Output	Non-028B models: Transceiver bank 1A Transmit Channel 0 (P) 028B model: Transceiver bank 1B Transmit Channel 0 (P)
C25	GND				Ground
C26	GND				Ground
C27	GTSL_1A_REFCLK_RX_N	REFCLK_GTSL_1A_RX_N / REFCLK_GTSL_1B_RX_N	P24	Input	Non-028B models: Transceiver bank 1A Regional Reference Clock (N) 028B model: Transceiver bank 1B Regional Reference Clock (N)
C28	GTSL_1A_REFCLK_RX_P	REFCLK_GTSL_1A_RX_P / REFCLK_GTSL_1B_RX_P	P25	Input	Non-028B models: Transceiver bank 1A Regional Reference Clock (P) 028B model: Transceiver bank 1B Regional Reference Clock (P)
C29	GND				Ground
C30	GND				Ground
C31	GTSL_1X_RX_CH2_N	NC / GTSL1A_RX_CH2N	AB29	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Receive Channel 2 (N)
C32	GTSL_1X_RX_CH2_P	NC / GTSL1A_RX_CH2P	AB30	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Receive Channel 2 (P)
C33	GND				Ground
C34	GND				Ground
C35	GTSL_1X_RX_CH0_N	NC / GTSL1A_RX_CH0N	AF30	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Receive Channel 0 (N)

Pin No.	CN2 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
C36	GTSL_1X_RX_CH0_P	NC / GTSL1A_RX_CH0P	AF29	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Receive Channel 0 (P)
C37	GND				Ground
C38	GND				Ground
C39	HVIO_5B_VCCIO	VCCIO_HVIO_5B	AB21	Power, Input	HVIO bank 5A VCCIO supply voltage (1.8-3.3V)
C40	HVIO_5B_VCCIO	VCCIO_HVIO_5B	AC21	Power, Input	HVIO bank 5A VCCIO supply voltage (1.8-3.3V)
C41	HVIO_5B_IO15	HVIO_5B_15	AH28	I/O	HVIO bank 5B single-ended I/O
C42	HVIO_5B_IO17	HVIO_5B_17	AF27	I/O	HVIO bank 5B single-ended I/O
C43	GND				Ground
C44	HVIO_5B_IO20	HVIO_5B_20	AK27	I/O	HVIO bank 5B single-ended I/O
C45	HVIO_5B_IO10	HVIO_5B_10	AH27	I/O	HVIO bank 5B single-ended I/O
C46	HVIO_5B_IO7	HVIO_5B_7	AK25	I/O	HVIO bank 5B single-ended I/O
C47	HVIO_5B_IO2	HVIO_5B_2	AH26	I/O	HVIO bank 5B single-ended I/O
C48	GND				Ground
C49	HVIO_5B_IO5	HVIO_5B_5	AG26	I/O	HVIO bank 5B single-ended I/O
C50	HVIO_5B_IO4	HVIO_5B_4	AH25	I/O	HVIO bank 5B single-ended I/O
C51	HVIO_5B_IO6	HVIO_5B_6	AE25	I/O	HVIO bank 5B single-ended I/O
C52	HVIO_5B_IO19	HVIO_5B_19	AK21	I/O	HVIO bank 5B single-ended I/O
C53	GND				Ground
C54	SOM_PWR_OK_3V3			Output	SoM Power OK signal
C55	SOM_PWR_EN_3V3			Input	SoM Power Enable signal
C56	GND				Ground
C57	GND				Ground
C58	SOM_VIN			Power, Input	SoM supply voltage
C59	SOM_VIN			Power, Input	SoM supply voltage
C60	SOM_VIN			Power, Input	SoM supply voltage
D1	HPS_RGMII_RXD3_1V8	HPS_IOB_24 / EMAC2_RXD3	C16	I/O, Input	HPS IOB bit 24 / EMAC2 Receive Data bit 3
D2	HPS_RGMII_RXD0_1V8	HPS_IOB_19 / EMAC2_RXD0	D17	I/O, Input	HPS IOB bit 19 / EMAC2 Receive Data bit 0
D3	HPS_RGMII_RXD2_1V8	HPS_IOB_23 / EMAC2_RXD2	C17	I/O, Input	HPS IOB bit 23 / EMAC2 Receive Data bit 2
D4	HPS_RGMII_RXD1_1V8	HPS_IOB_20 / EMAC2_RXD1	A19	I/O, Input	HPS IOB bit 20 / EMAC2 Receive Data bit 1
D5	GND				Ground
D6	HPS_RGMII_RX_CTRL_1V8	HPS_IOB_16 / EMAC2_RX_CTL	B20	I/O, Input	HPS IOB bit 16 / EMAC2 Receive Control
D7	HPS_RGMII_RX_CLK_1V8	HPS_IOB_15 / EMAC2_RX_CLK	E19	I/O, Input	HPS IOB bit 15 / EMAC2 Receive Clock
D8	HPS_I2C_SCL_1V8	HPS_IOA_10 / I2C_EMAC1_SCL	D22	I/O	HPS IOA bit 10 / I2C Serial Clock
D9	HPS_I2C_SDA_1V8	HPS_IOA_9 / I2C_EMAC1_SDA	C26	I/O	HPS IOA bit 9 / I2C Serial Data
D10	GND				Ground
D11	HPS_IOA12_1V8	HPS_IOA_12	A26	I/O	HPS IOA bit 12
D12	HPS_IOA11_1V8	HPS_IOA_11	A23	I/O	HPS IOA bit 11
D13	HPS_1PPS_IN_1V8	HPS_IOA_6 / EMAC2_PPSTRIG2	F23	I/O, Input	HPS IOA bit 6 / EMAC2 1PPS Trigger signal
D14	HPS_1PPS_OUT_1V8	HPS_IOA_5 / EMAC2_PPS2	B28	I/O, Output	HPS IOA bit 5 / EMAC2 1PPS signal
D15	RESERVED				Internally unconnected reserved pin
D16	GND				Ground
D17	RESERVED				Internally unconnected reserved pin
D18	RESERVED				Internally unconnected reserved pin
D19	GND				Ground
D20	GND				Ground
D21	GTSL_1A_RX_CH2_N	GTSL1A_RX_CH2N / GTSL1B_RX_CH2N	F29	Input	Non-028B models: Transceiver bank 1A Receive Channel 2 (N) 028B model: Transceiver bank 1B Receive Channel 2 (N)

Pin No.	CN2 Signal Name	FPGA Pin Name	FPGA Pin No.	I/O	Description
D22	GTSL_1A_RX_CH2_P	GTSL1A_RX_CH2P / GTSL1B_RX_CH2P	F30	Input	Non-028B models: Transceiver bank 1A Receive Channel 2 (P) 028B model: Transceiver bank 1B Receive Channel 2 (P)
D23	GND				Ground
D24	GND				Ground
D25	GTSL_1A_RX_CH0_N	GTSL1A_RX_CH0N / GTSL1B_RX_CH0N	K29	Input	Non-028B models: Transceiver bank 1A Receive Channel 0 (N) 028B model: Transceiver bank 1B Receive Channel 0 (N)
D26	GTSL_1A_RX_CH0_P	GTSL1A_RX_CH0P / GTSL1B_RX_CH0P	K30	Input	Non-028B models: Transceiver bank 1A Receive Channel 0 (P) 028B model: Transceiver bank 1B Receive Channel 0 (P)
D27	GND				Ground
D28	GND				Ground
D29	GTSL_1X_TX_CH2_N	NC / GTSL1A_TX_CH2N	V28	Output	Non-028B models: Not connected 028B model: Transceiver bank 1A Transmit Channel 2 (N)
D30	GTSL_1X_TX_CH2_P	NC / GTSL1A_TX_CH2P	V29	Output	Non-028B models: Not connected 028B model: Transceiver bank 1A Transmit Channel 2 (P)
D31	GND				Ground
D32	GND				Ground
D33	GTSL_1X_TX_CH0_N	NC / GTSL1A_TX_CH0N	AC27	Output	Non-028B models: Not connected 028B model: Transceiver bank 1A Transmit Channel 0 (N)
D34	GTSL_1X_TX_CH0_P	NC / GTSL1A_TX_CH0P	AD27	Output	Non-028B models: Not connected 028B model: Transceiver bank 1A Transmit Channel 0 (P)
D35	GND				Ground
D36	GND				Ground
D37	GTSL_1X_REFCLK_RX_N	NC / REFCLK_GTSL_1A_RX_N	Y24	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Regional Reference Clock (N)
D38	GTSL_1X_REFCLK_RX_P	NC / REFCLK_GTSL_1A_RX_P	Y25	Input	Non-028B models: Not connected 028B model: Transceiver bank 1A Regional Reference Clock (P)
D39	GND				Ground
D40	RESERVED				Internally unconnected reserved pin
D41	RESERVED				Internally unconnected reserved pin
D42	HVIO_5B_IO13	HVIO_5B_13	AJ29	I/O	HVIO bank 5B single-ended I/O
D43	HVIO_5B_IO18	HVIO_5B_18	AJ28	I/O	HVIO bank 5B single-ended I/O
D44	GND				Ground
D45	HVIO_5B_IO9	HVIO_5B_9	AJ27	I/O	HVIO bank 5B single-ended I/O
D46	HVIO_5B_IO14	HVIO_5B_14	AK26	I/O	HVIO bank 5B single-ended I/O
D47	HVIO_5B_IO3	HVIO_5B_3	AJ25	I/O	HVIO bank 5B single-ended I/O
D48	HVIO_5B_IO1	HVIO_5B_1	AK24	I/O	HVIO bank 5B single-ended I/O
D49	GND				Ground
D50	HVIO_5B_IO12	HVIO_5B_12	AK22	I/O	HVIO bank 5B single-ended I/O
D51	HVIO_5B_IO8	HVIO_5B_8	AF26	I/O	HVIO bank 5B single-ended I/O
D52	HVIO_5B_IO16	HVIO_5B_16	AK20	I/O	HVIO bank 5B single-ended I/O
D53	HVIO_5B_IO11	HVIO_5B_11	AK19	I/O	HVIO bank 5B single-ended I/O
D54	GND				Ground
D55	RESERVED				Internally unconnected reserved pin
D56	RESERVED				Internally unconnected reserved pin
D57	GND				Ground
D58	SOM_VIN			Power, Input	SoM supply voltage
D59	SOM_VIN			Power, Input	SoM supply voltage
D60	SOM_VIN			Power, Input	SoM supply voltage

3. **Electrical Specifications**

3.1. Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Condition	Min	Max	Unit	Note
SOM	VIN	-	-0.3	13.2	V	SOM_VIN
VCCIO voltage	VHSIO	VCCIO=1.2V	-0.5	1.64	V	Bank_2A_T_VCCIO Bank_2A_B_VCCIO
		VCCIO=1.3V	-0.5	1.74	V	
	VHVIO VHVIO	VCCIO=1.8V	-0.5	2.04	V	HVIO_5A_VCCIO HVIO_5B_VCCIO
		VCCIO=2.5V	-0.5	2.83	V	
		VCCIO=3.3V	-0.5	3.74	V	
VCCBAT voltage	VCCBAT	-	-0.5	2.08	V	1.8_VCCBAT
Input voltage	VI_HPS	-	-0.3	2.38	V	HPS
	VI_SDM	-	-0.3	2.38	V	SDM
	VI_HSIO	-	-0.3	VHSIO+0.25	V	HSIO
	VI_HVIO	-	-0.3	VHVIO+0.3	V	HVIO
	VI_18	-	-0.3	2.38	V	Signals with suffix _1V8 except for the above
	VI_33	-	-0.3	6	V	SOM_PWR_EN_3V3
Operating temperature	Topr	-	-25	85	°C	No condensation

3.2. Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Power supply voltage	VIN	-	4.75	5.0	13.2	V	SOM_VIN
HSIO VCCIO Voltage	VHSIO	VCCIO=1.2V	1.164	1.2	1.236	V	Bank_2A_T_VCCIO Bank_2A_B_VCCIO
		VCCIO=1.3V	1.261	1.3	1.339	V	
HVIO VCCIO voltage	VHVIO	VCCIO=1.8V	1.746	1.8	1.854	V	HVIO_5A_VCCIO HVIO_5B_VCCIO
		VCCIO=2.5V	2.425	2.5	2.575	V	
		VCCIO=3.3V	3.201	3.3	3.399	V	
VCCBAT volage	VCCBAT	-	1	1 - 1.8	1.8	V	1.8_VCCBAT
Input voltage	HPS_VI	-	-0.3	1.8	2.1	V	HPS
	SDM_VI	-	-0.3	1.8	2.1	V	SDM
	HSIO11_VI	-	-0.3	1.1	1.35	V	HSIO (Bank3AT)
	HSIO_VI	-	-0.3		VHSIO+0.25	V	HSIO
	HVIO_VI	-	-0.3		VHVIO+0.3	V	HVIO
	VI_18	-	-0.3	1.8	2.1	V	Signals with suffix _1V8 except for the above
	VI_33	-	-0.3	3.3	3.6	V	SOM_PWR_OK_3V3 SOM_PWR_EN_3V3

3.3. IO Pin Specifications

IO Pin Specifications vary depending on bank voltage and configuration settings. For details, please refer to the datasheet for the latest Agilex™ 5 FPGA & SoC E-Series.

4. Mechanical Dimensions

The dimensional detail of this product is shown below. (Unit: mm)

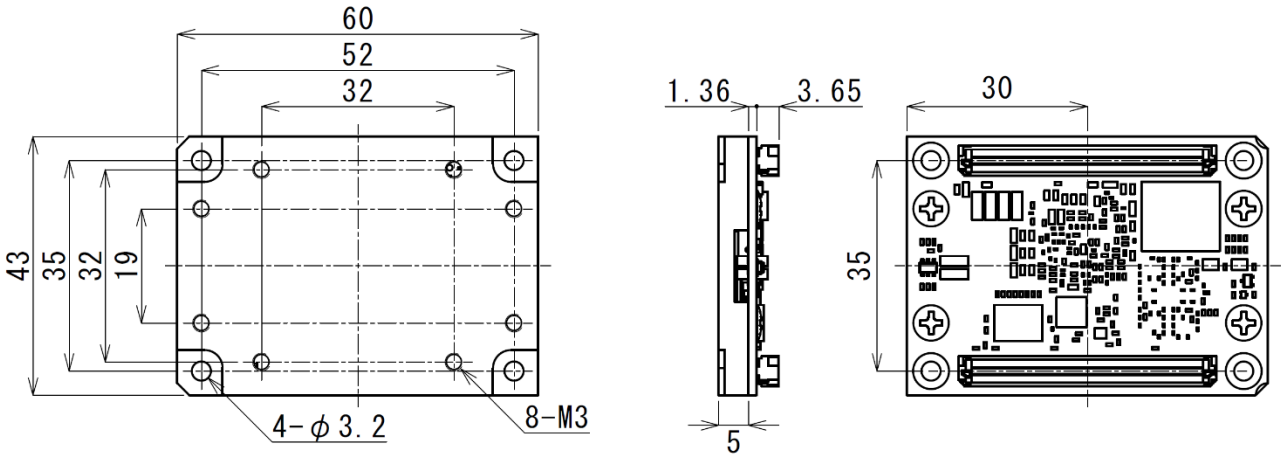


Figure 3-1 Mechanical Dimensions (with heat spreader)

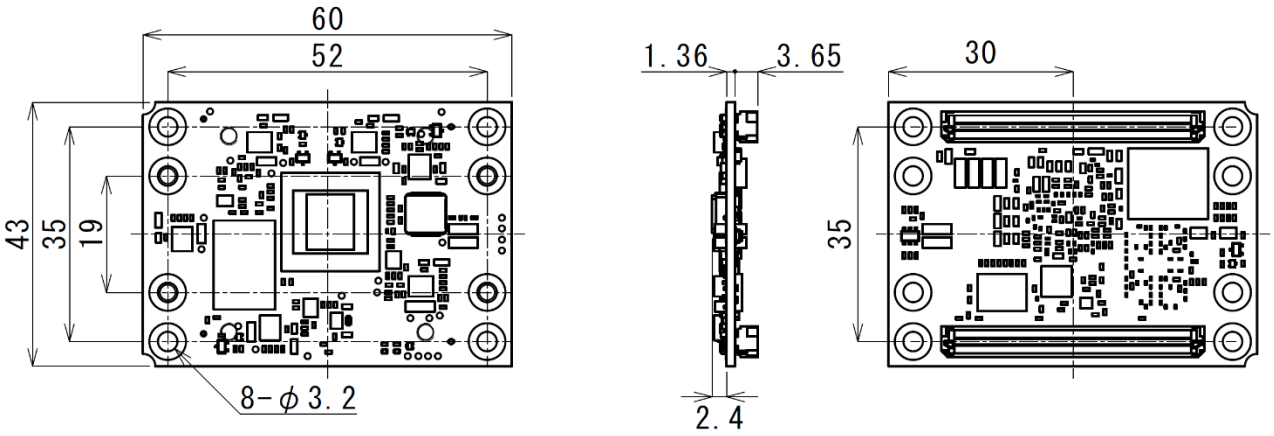


Figure 3-2 Mechanical Dimensions (without heat spreader)

5. Document History

Ver.	Date	Description
1.0	2026/05/11	Initial release.